

ACL10 LA-1331 Schematics Document

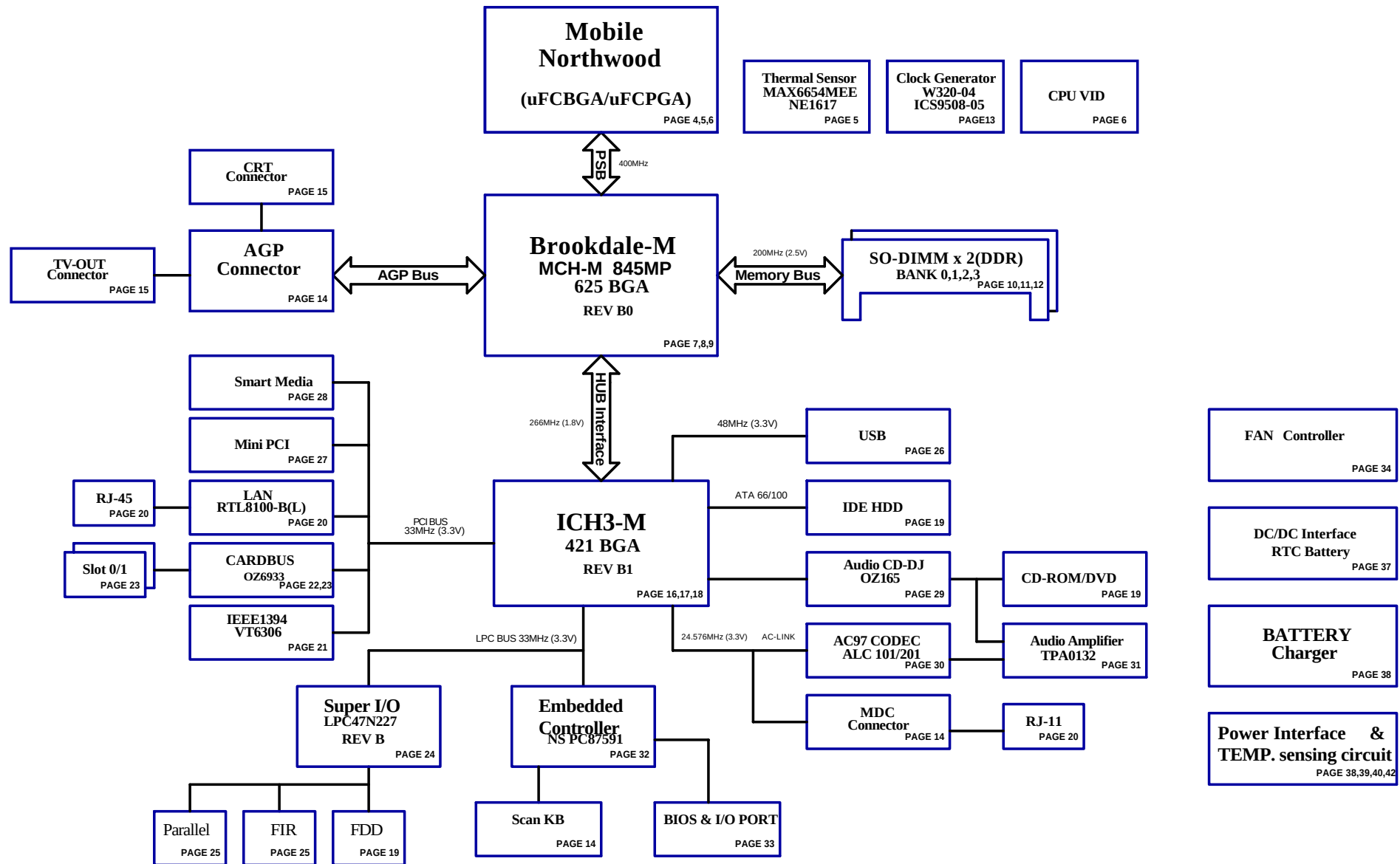
REV 2.0 (For 030)

INTEL Mobile P4 uFCBGA/uFCPGA Northwood
MCH-M(845-MP) + ICH3-M + SQ17

COMPAL ELECTRONICS, INC			
Title			
Schematic MB LA-1331			
Size	Document Number		Rev
Custom	401207		2A
Date:	星期四, 三月 18, 2004		Sheet 1 of 83

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ACL10 LA-1331 BLOCK DIAGRAM



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
1.2VP	1.2VP switched power rail for CPU VID	ON	OFF	OFF
+1.25VS	1.25VS power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V always power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON
+SDREF	+SDREF power	ON	ON	OFF

Note : "ON"" means that this power plane is "ON" only with AC power available, otherwise it is "OFF".

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
IEEE 1394	AD16	0	PIRQA
Mini-PCI	AD18	1/4	PIRQC/PIRQD
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
SM	AD22	-	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	MAX6654MEE	1001 110Xb
EEPROM(24C16/02)	1010 000Xb	OZ165	1011 0100b (B4h)
(24C04)	1011 000Xb	Smart Battery	0001 011Xb
		Docking	0011 011Xb
		DOT Board	XXXX XXXXb

EC SM Bus2 address

ICH3-M SM Bus address

Device	Address
Clock Generator W320-04 / ICS9508-05	1101 0000

DDR SODIMM SM Bus address

DDR SLOT	SA2	SA1	SA0
DDR SODIMM0 (REVERSE)	0	0	0
DDR SODIMM1 (NORMAL)	0	0	1

PIR

REV 0.1

Date	Page	Description
2001/12/29	7	Change R212,R214 & R213 to 8.2K ohm for Intel recommend
2001/12/29	14	Stuff R361=22 Ohm and no-stuff R360 for Data-IN1 of MDC module.
2001/12/29	15	Change L28 & L29 to 0 Ohm for EMI issue.
2001/12/29	16	Change R39 power-plane to +3VALW for Resume-well Power-plane(+3VALW)
2001/12/29	17	DEL C73, C87, C371 for EMI issue.
2001/12/29	17	Change L37 power-plane to +1.8VS for Intel recommend.
2001/12/29	17	Change R279 power-plane to +3VS for Intel recommend.
2001/12/29	17	Change U29 pinV22,U18 & P14 power-plane to +CPU_CORE for Intel recommend.
2001/12/29	17	Change R284 power-plane to +3VALW for Intel recommend.
2001/12/29	18	Change "SMB_ALERT#" power-plane to +3VALW for "RESUME-WELL" power-plane(+3VLAW).
2001/12/29	18	Exchang D13,D14,D16,D17,D18 and R28,R34,R30,R29 to RP135,R466,R468 for cost-down.
2001/12/29	20	Add D43 for leakage.
2001/12/29	21	Exchang L42 to L52,L53, L54, L55 for ME limitation.
2001/12/29	27	Add D42 for leakage.
2001/12/29	31	Add R465 for PC99 Spec.
2001/12/29	34	Add C368, C369 for EMI solution.
2001/12/29	35	EC control "EC_RSMRST#". ->DEL R92, Stuff R48.
2001/12/29	35	Change R97 to 100K for "VGATE" of Max1718A issue.-> Change PR134= 0 Ohm.
2002/01/07	39	Change PR68 from 10k_1% to 10.5k_1%.(increase 5valvp to 5.125v).
2002/01/07	40	Change PR81 from 2.15k_1% to 1.87k_1%.(CPU thermal OTP from 83+-3C to 85+-3C).
2002/01/07	42	Add PR147, PR161 to 2.7_0805. for EMI requirement.
2002/01/07	42	Add PC120, PC121, PC122 to 1000pf. for ESD.
2002/01/07	42	Add PQ44 to 2N7002 for CPU SPEED STEP.
2002/01/07	42	Change PR130, PR152 from 0 to 2.2. for EMI requirement.
2002/01/07	42	Change PR143 from 53.6k_1% to 100k_1%. for CPU OCP.
2002/01/07	42	Change PR145 from 100k_1% to 53.6k_1%. for CPU OCP.
2002/01/07	42	Change PR148 from 30k_1% to 48.7k_1%. for CPU OCP.
2002/01/07	42	Change PU12 VIN from +2.5VP to +3VALWP.

REV 0.2

Date	Page	Description
2002/01/11	40	Change PH1 and PH2 design by high active for AC-IN issue.

REV 0.3

Date	Page	Description
None		

REV 1.0

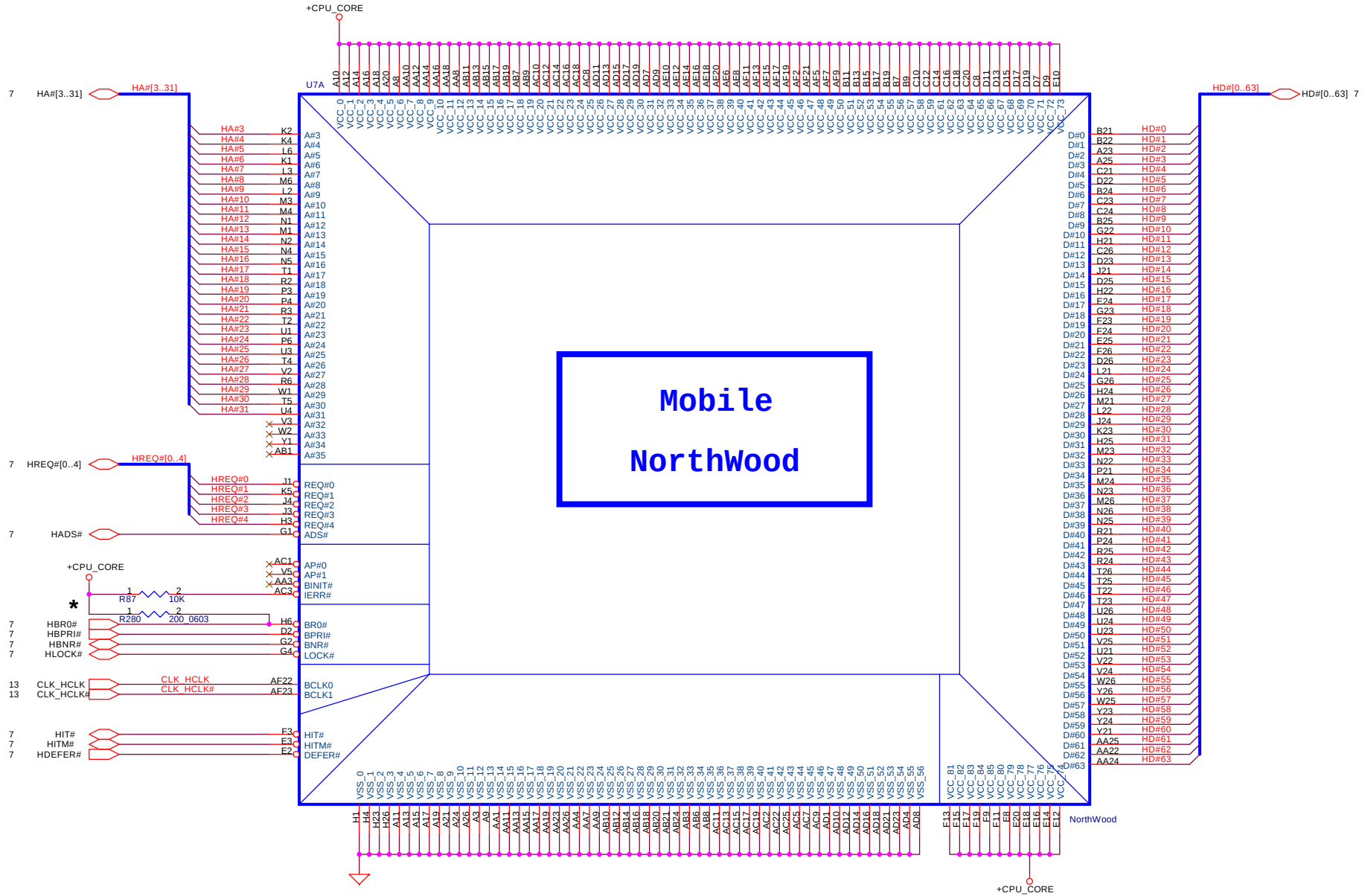
Date	Page
None	

REV 2.0

Date	Page	
2002/04/10	20	GCR: (For LAN Issue) <1>Isolation U18 pin6 for Realtek application notice. <2>Change R204 from 5.9K+-1% to 5.6K +-1%. <3>Change L23 from 4.7UH to 0 ohm.

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Size	Document Number		Rev
Custom	401207		2A
Date:	星期四, 三月 18, 2004	Sheet	3 of 83

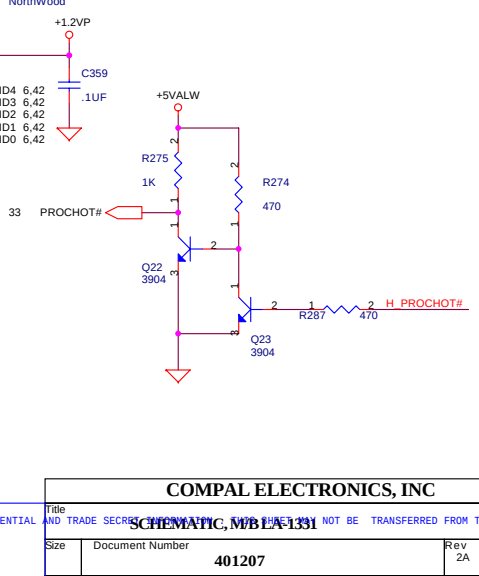
Mobile NorthWood



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Size	Custom	Document Number	401207
Date:	星期三, 三月 18, 2004	Sheet	4 of 83
Rev	2A		

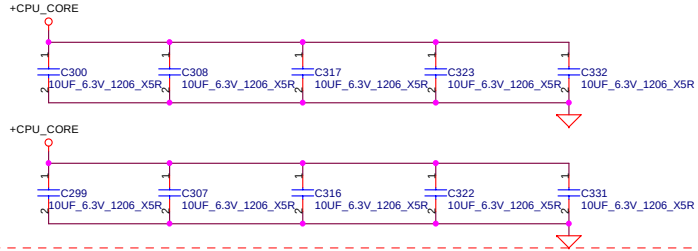
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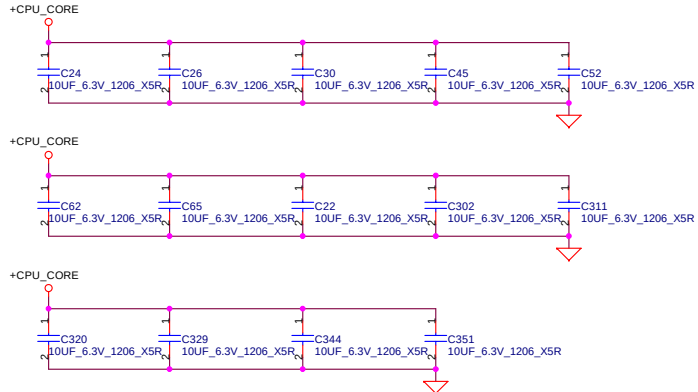
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

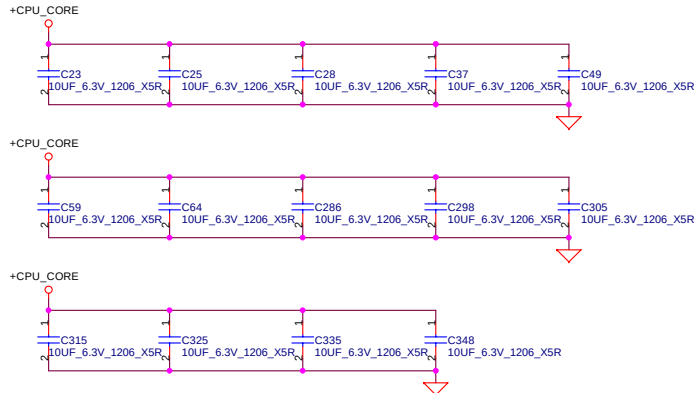
Please place these cap in the socket cavity area



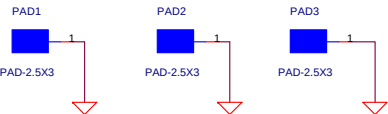
Please place these cap on the socket north side



Please place these cap on the socket south side



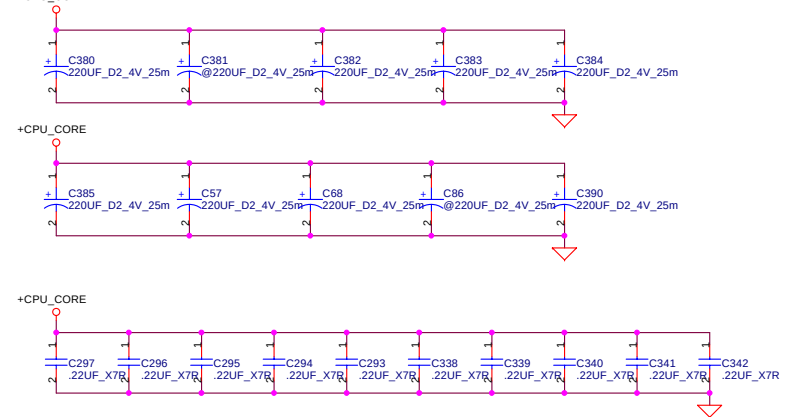
EMI Clip PAD for CPU



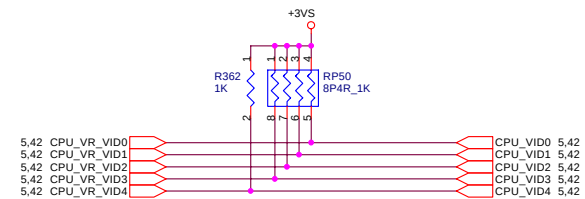
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm



CPU Voltage ID

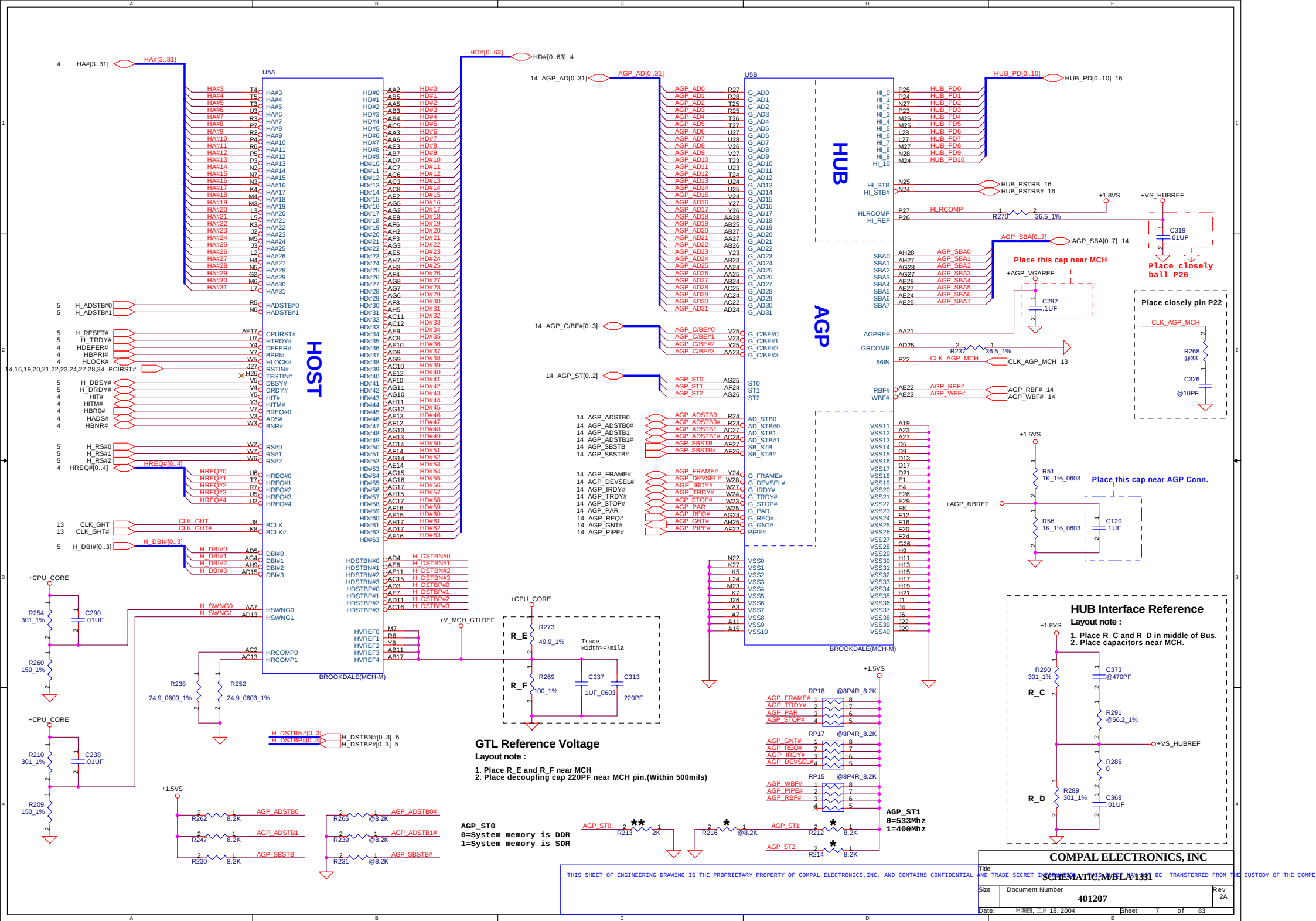


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Size	Document Number	Rev
	401207	2A
Date:	星期四, 三月 18, 2004	Sheet 6 of 83

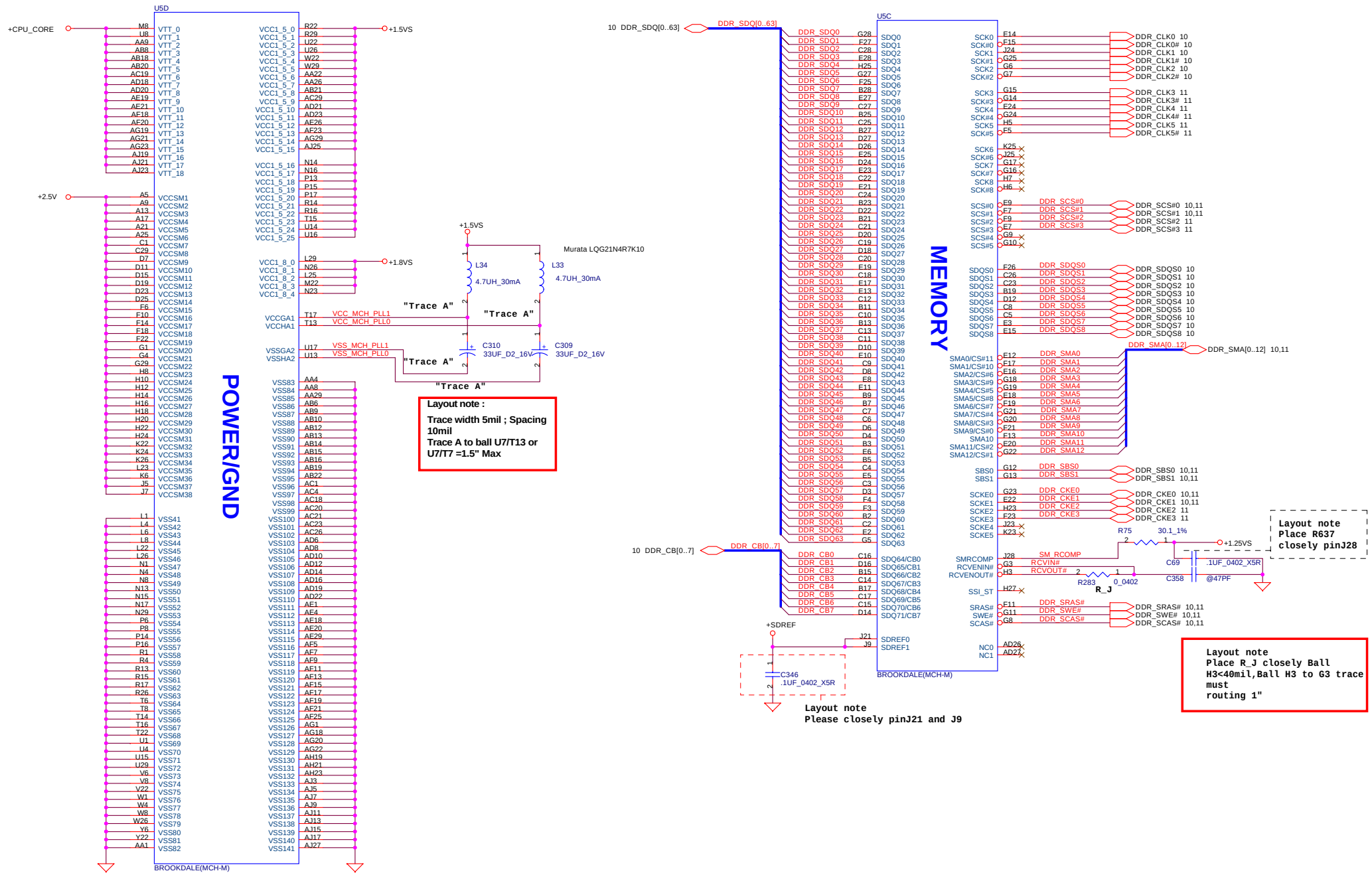


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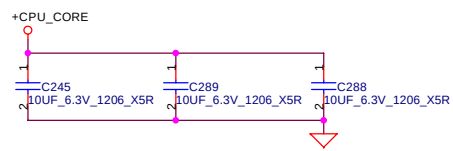
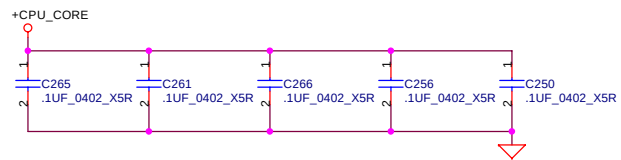
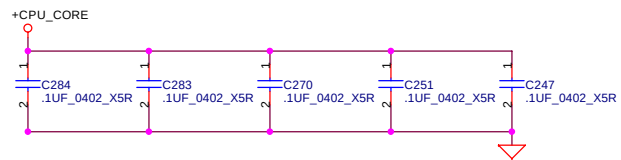
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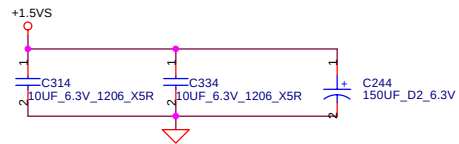
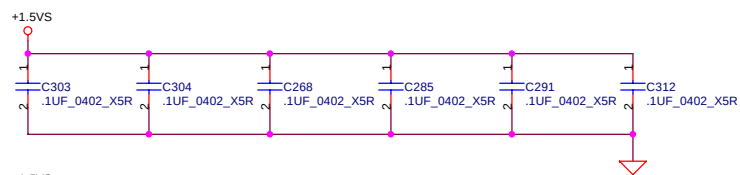
Date: 星期四, 三月 18, 2004 Sheet 7 of 83



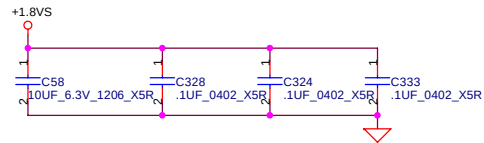
Layout note : Processor system bus
Distribute as close as possible
to MCH Processor Quadrant.(between VTTFSB and VSS pin)



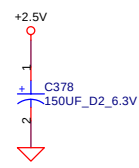
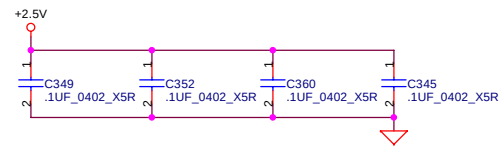
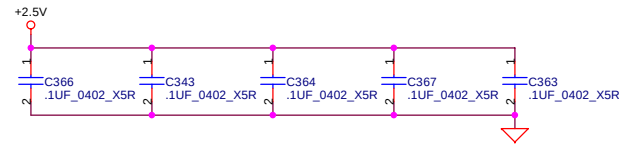
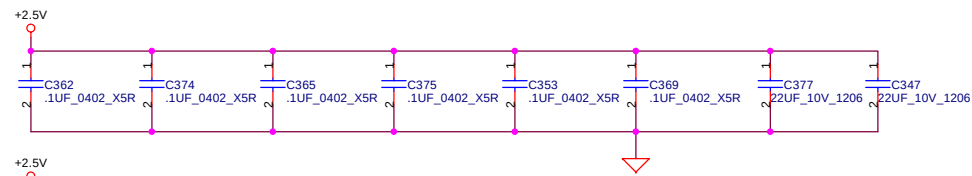
Layout note : AGP/CORE
Distribute as close as possible
to MCH Processor Quadrant.(between VCCAGP/VCCCORE
and VSS pin)



Layout note : Hub-Link
Distribute as close as possible
to MCH Processor Quadrant.(between VCCHL and VSS pin)



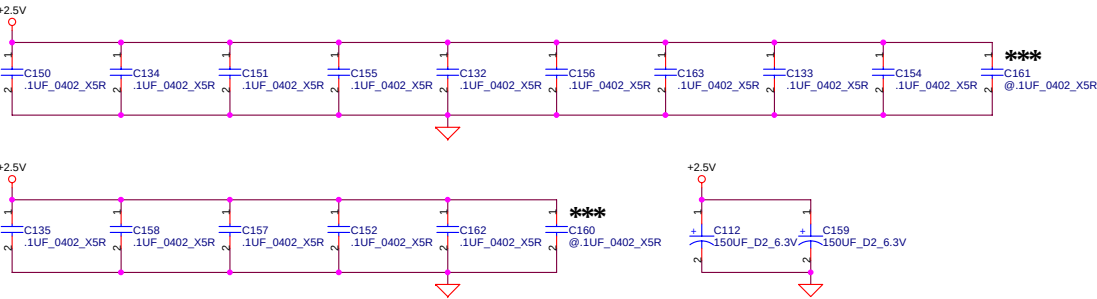
Layout note : DDR Memory interface
Distribute as close as possible
to MCH Processor Quadrant.(between VCCSM and VSS pin)







Layout note :
Distribute as close as possible
to DDR-SODIMM.



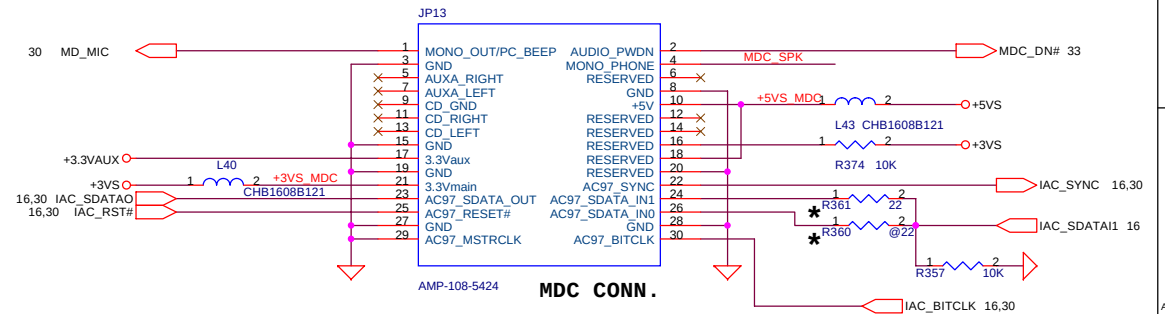
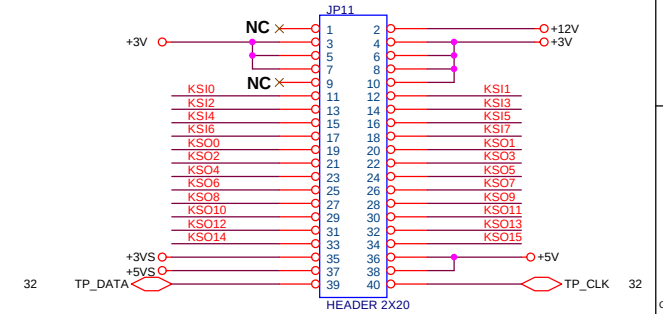
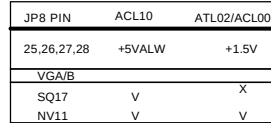
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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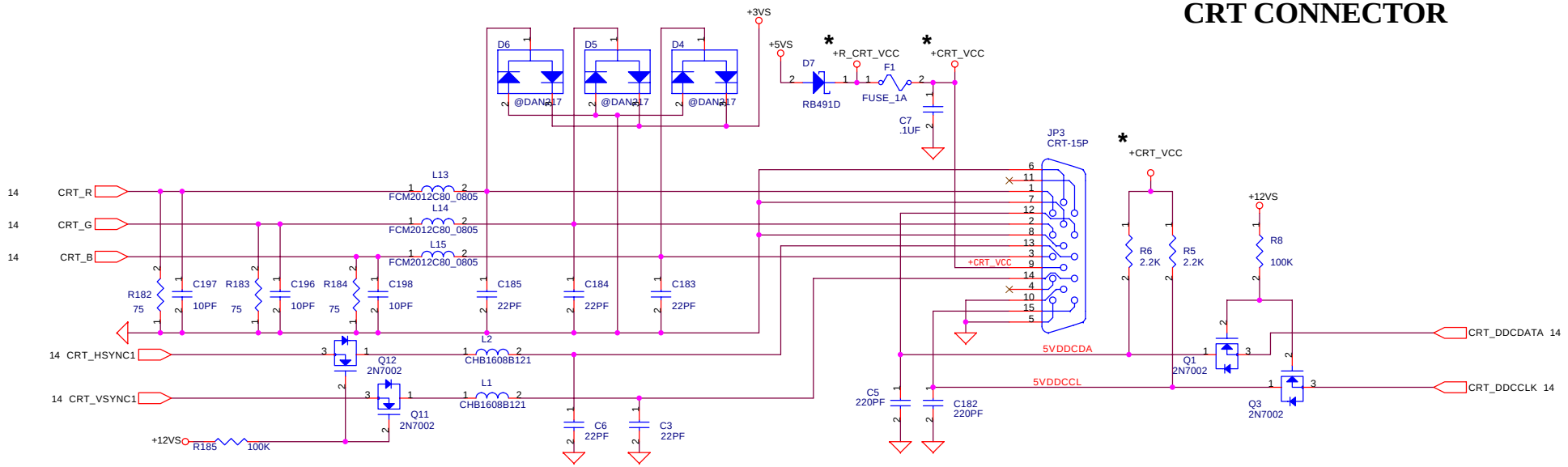
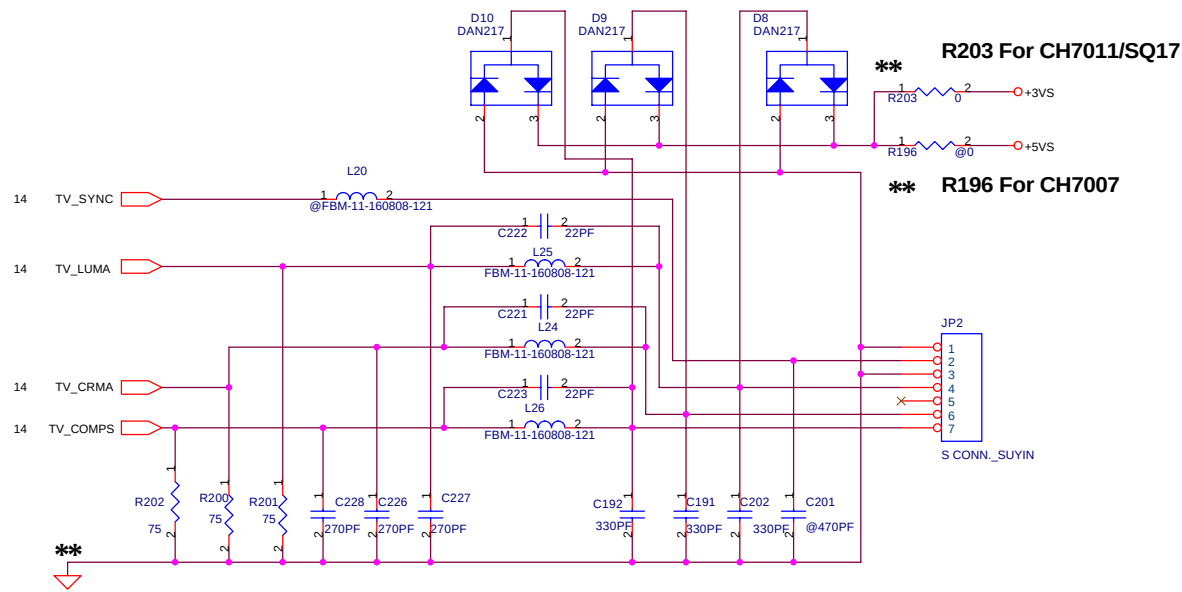
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Size		Document Number	
		401207	
Date:		Rev	
星期四, 三月 18, 2004		2A	
Sheet		of	
12		83	

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Date:	星期四, 三月 18, 2004	Sheet	14	of	83
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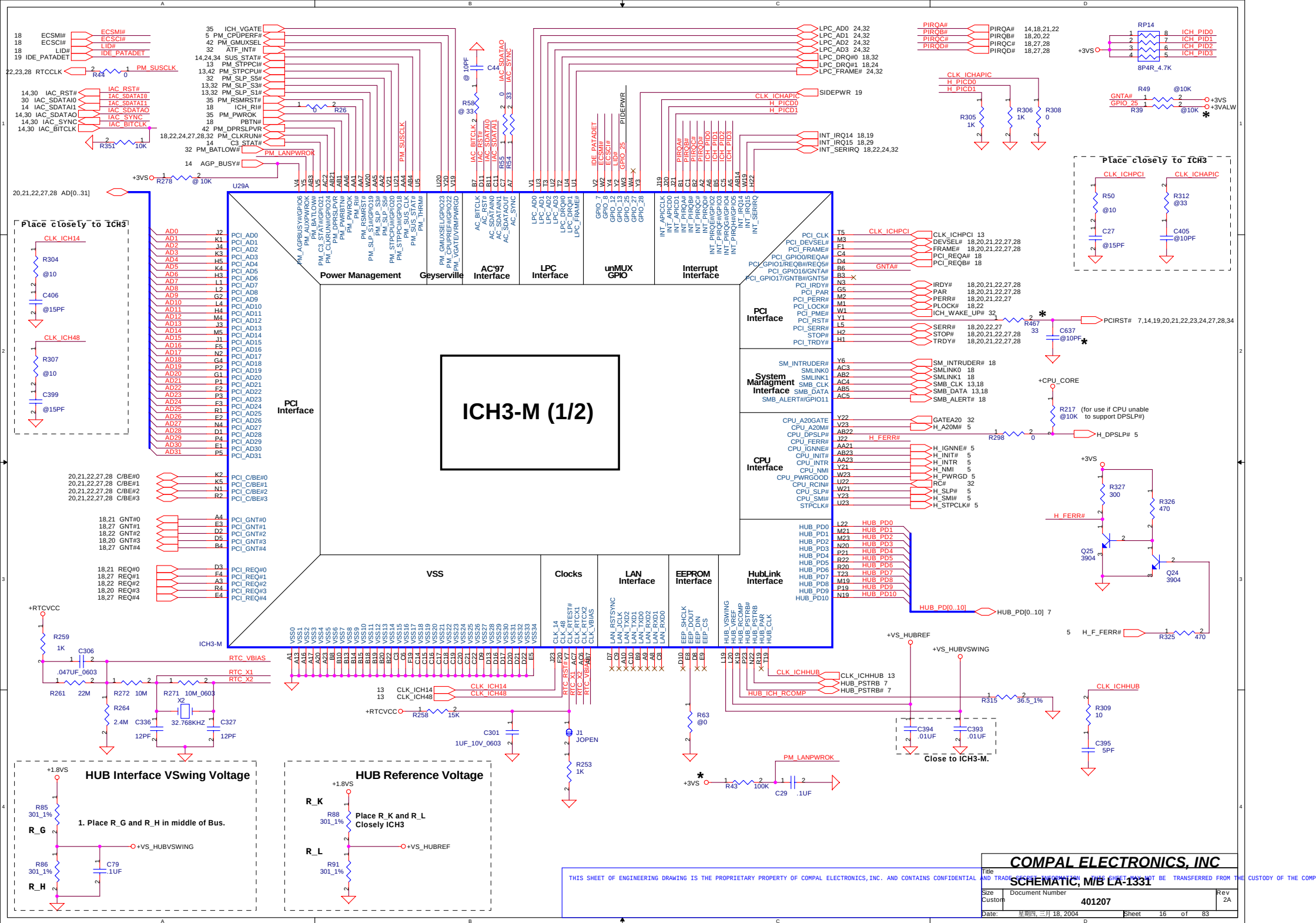
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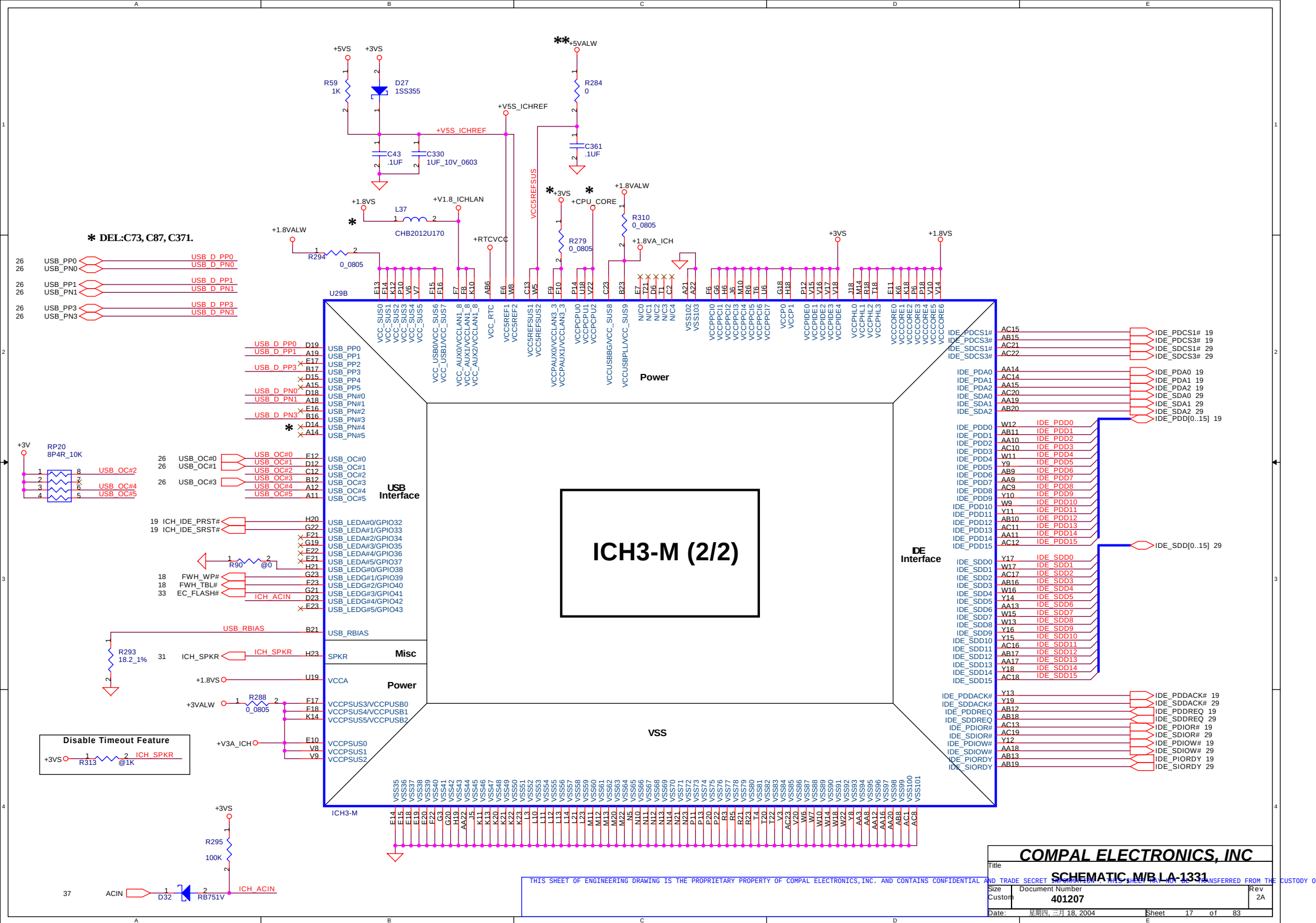
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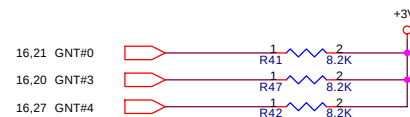
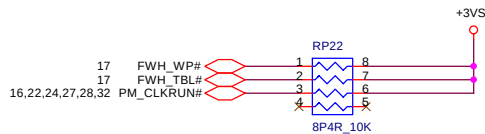
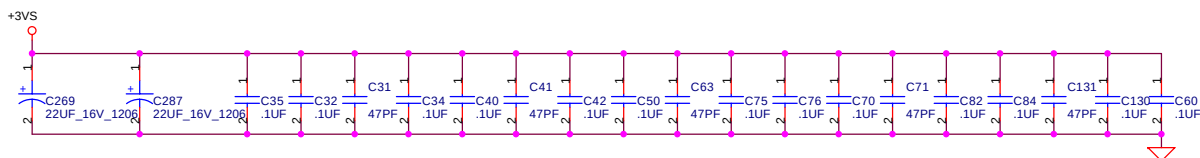
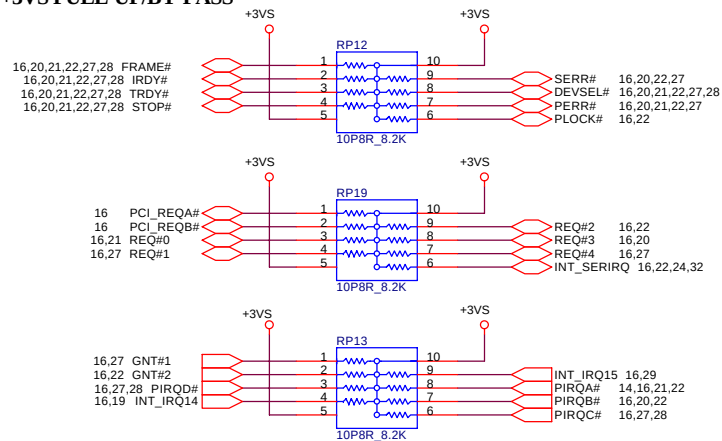
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Sheet 15 of 83

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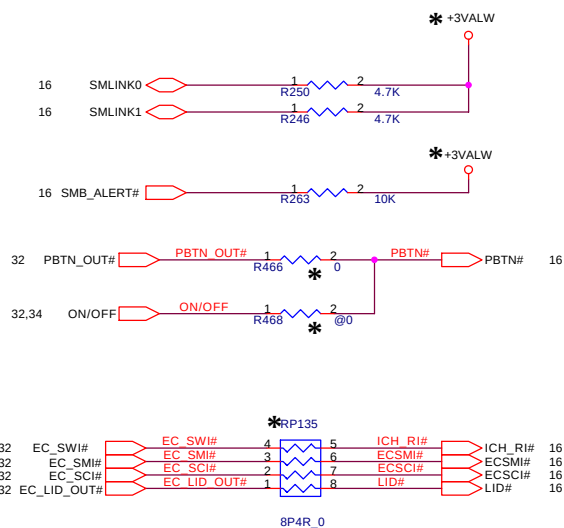




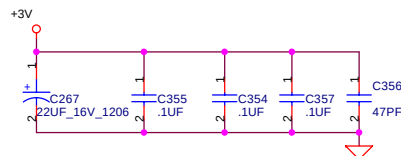
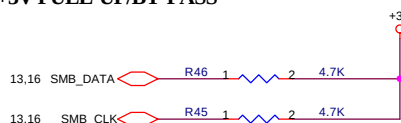
+3VS PULL-UP/BY-PASS



+3VALW PULL-UP



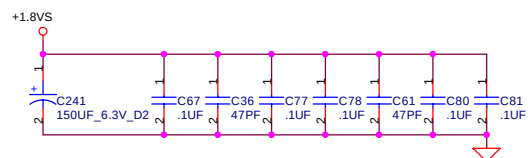
+3V PULL-UP/BY-PASS



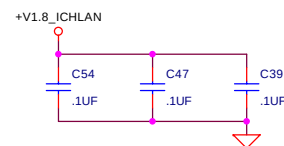
+RTCVCC PULL-UP



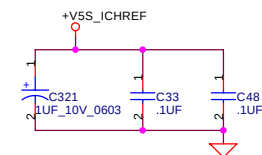
+1.8SV BY-PASS



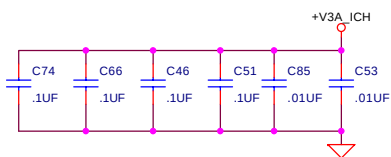
+V1.8S_ICHLAN BY-PASS



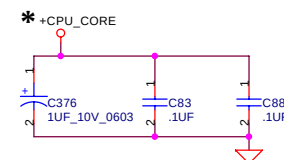
+V5S_ICHREF BY-PASS



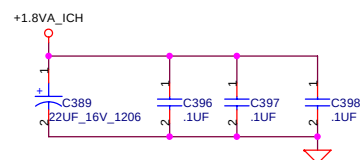
+V3A_ICH BY-PASS



+CPU_CORE BY-PASS



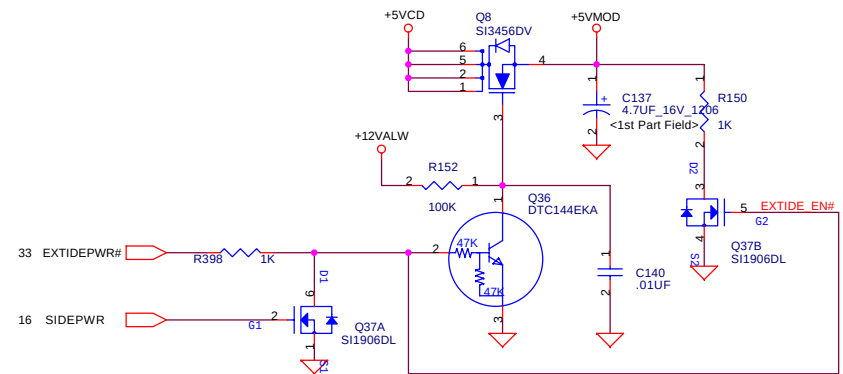
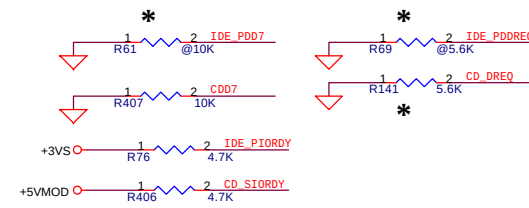
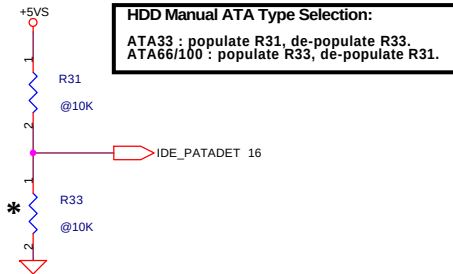
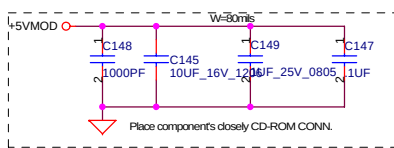
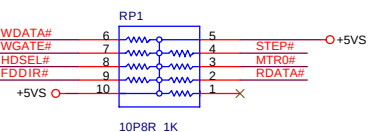
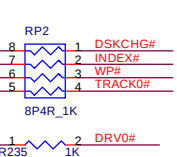
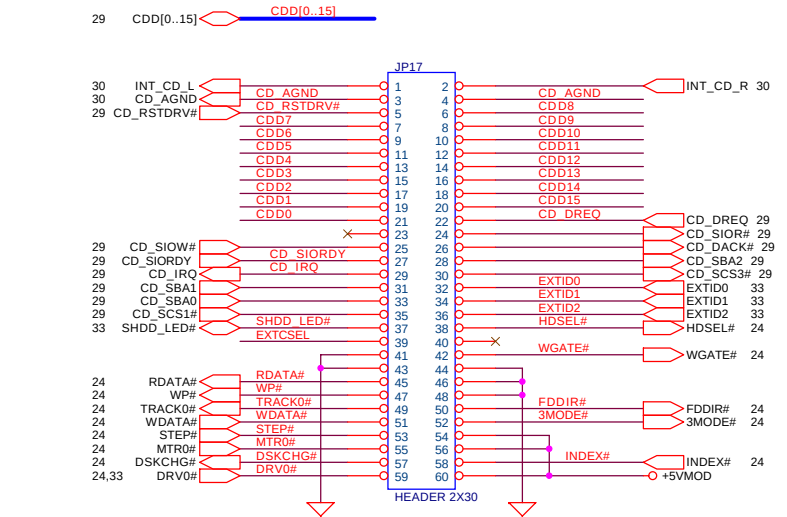
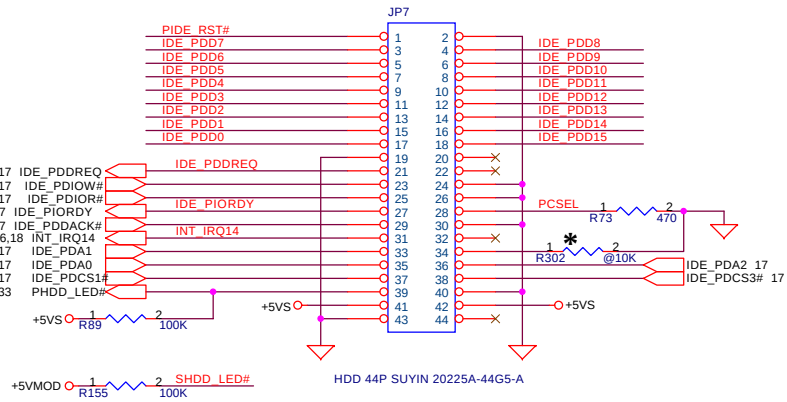
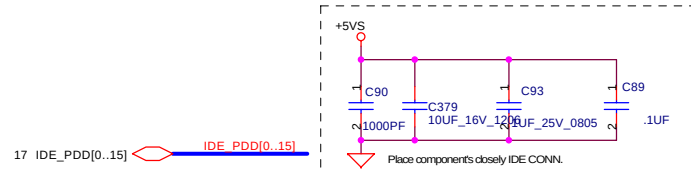
+1.8VA_ICH BY-PASS



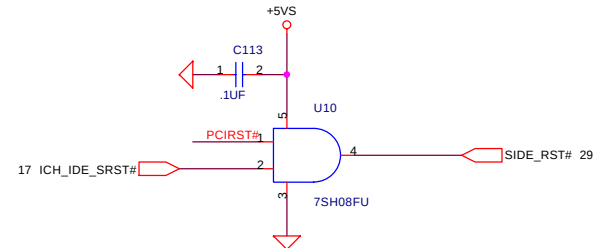
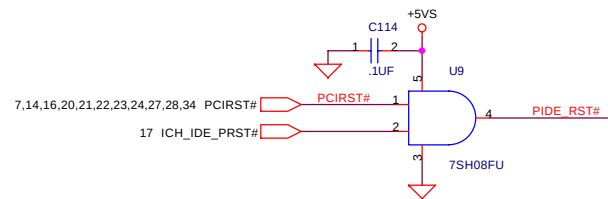
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Size	Document Number
Custom	401207
Date:	星期四, 三月 18, 2004
Sheet	18 of 83
Rev	2A

IDE,CD-ROM Module CONN.



SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

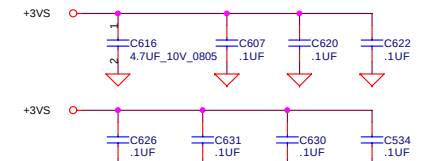
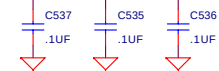
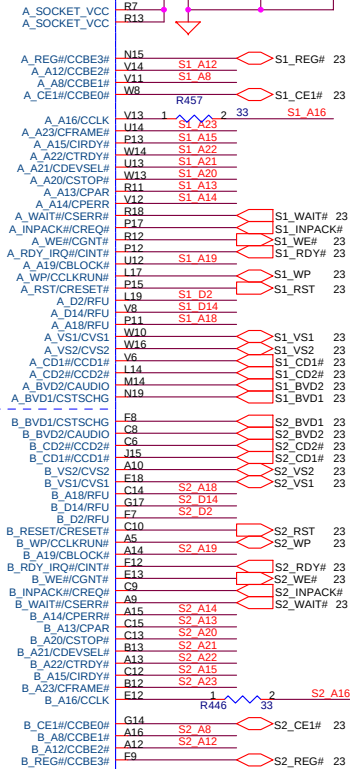
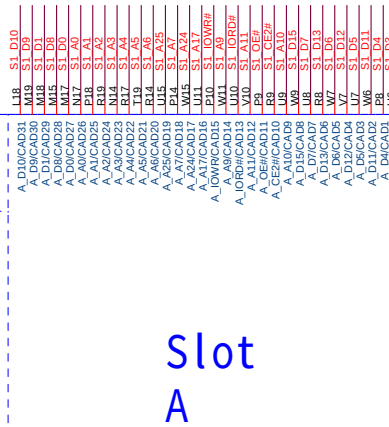
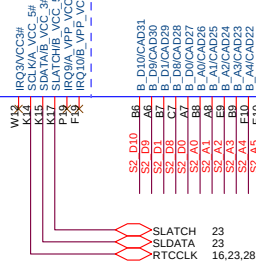
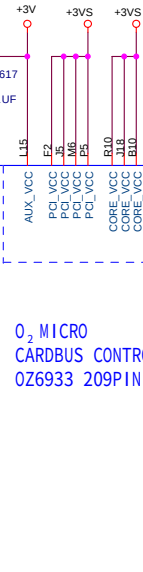
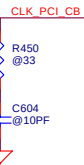
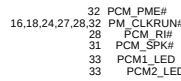
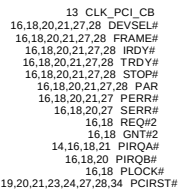
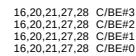


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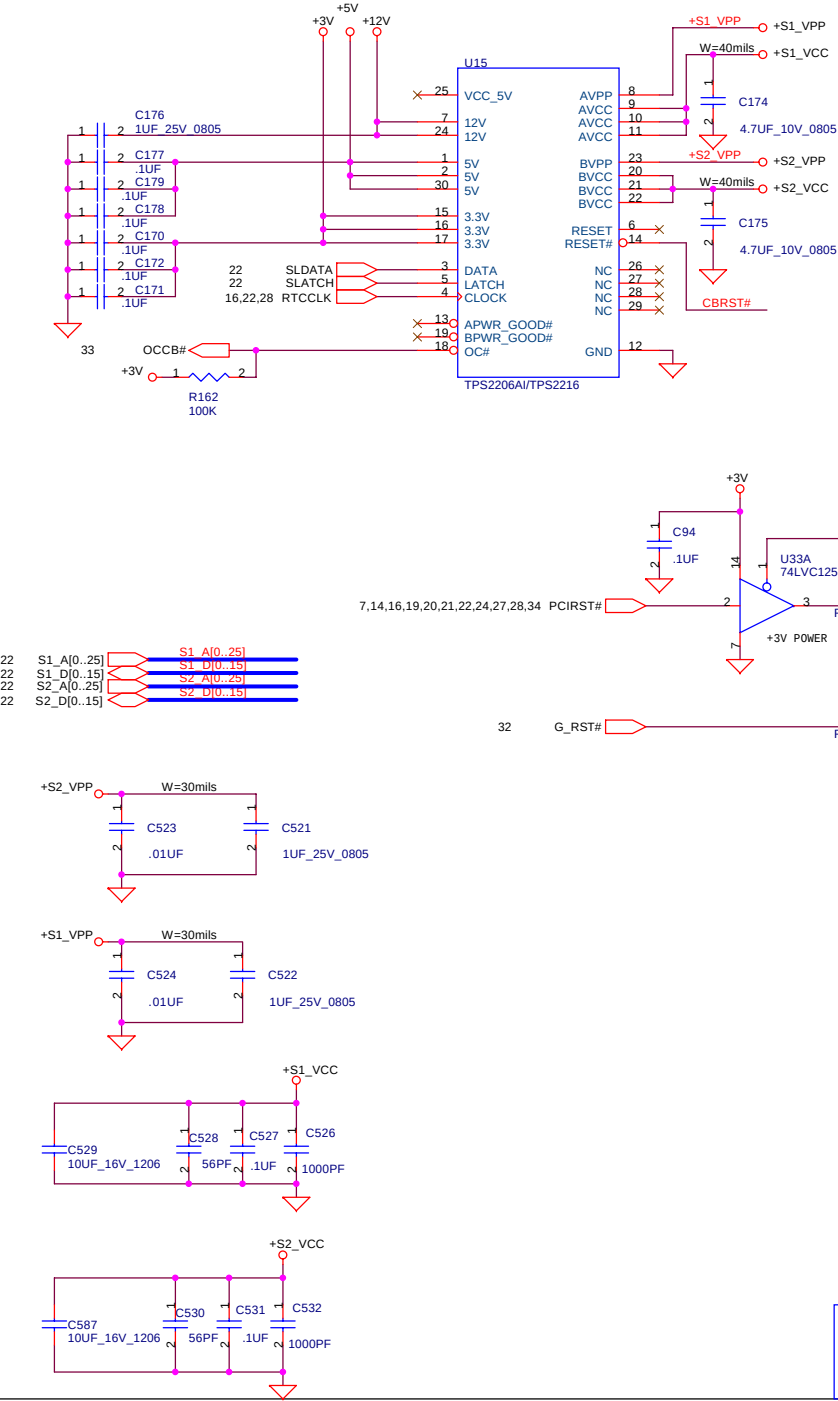
COMPAL ELECTRONICS, INC		
Title	SCHEMATIC, M/B LA-1331	
Size B	Document Number	Rev 2A
	401207	
Date:	星期四, 三月 18, 2004	Sheet 19 of 83



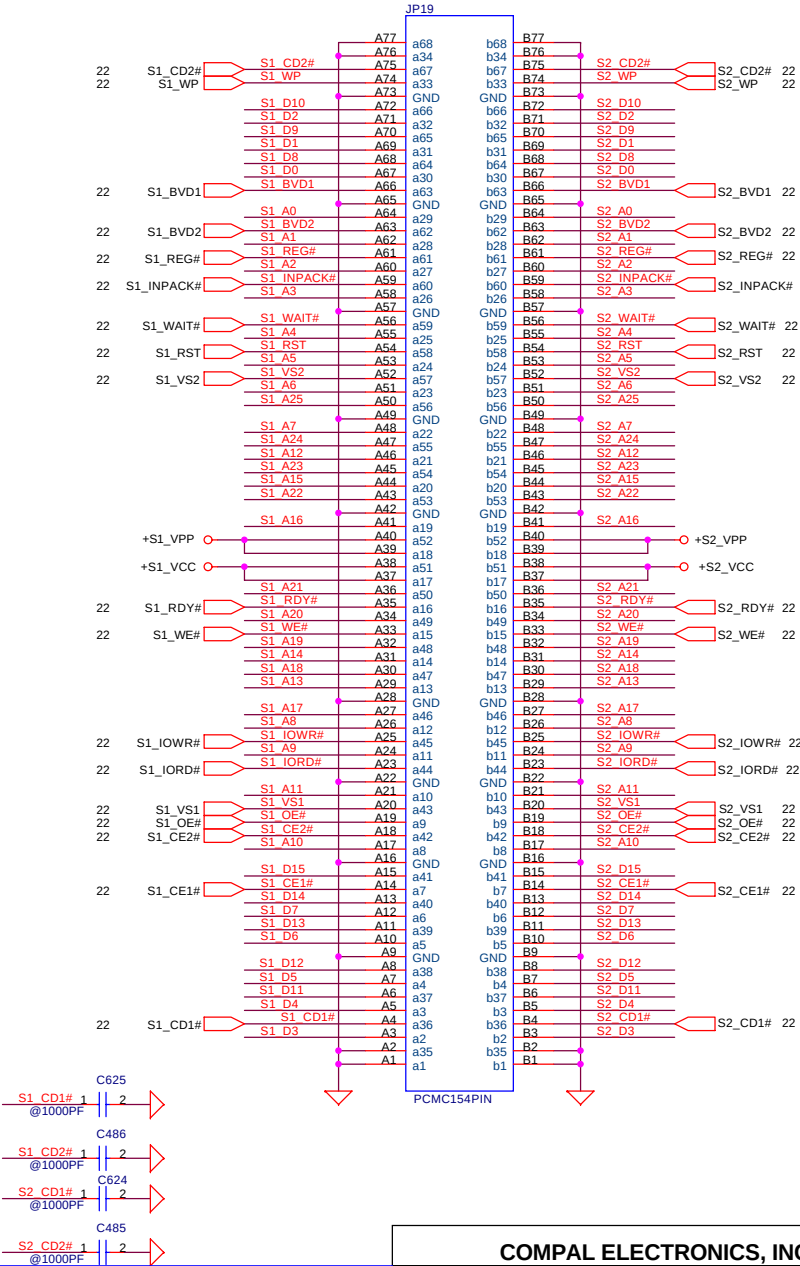
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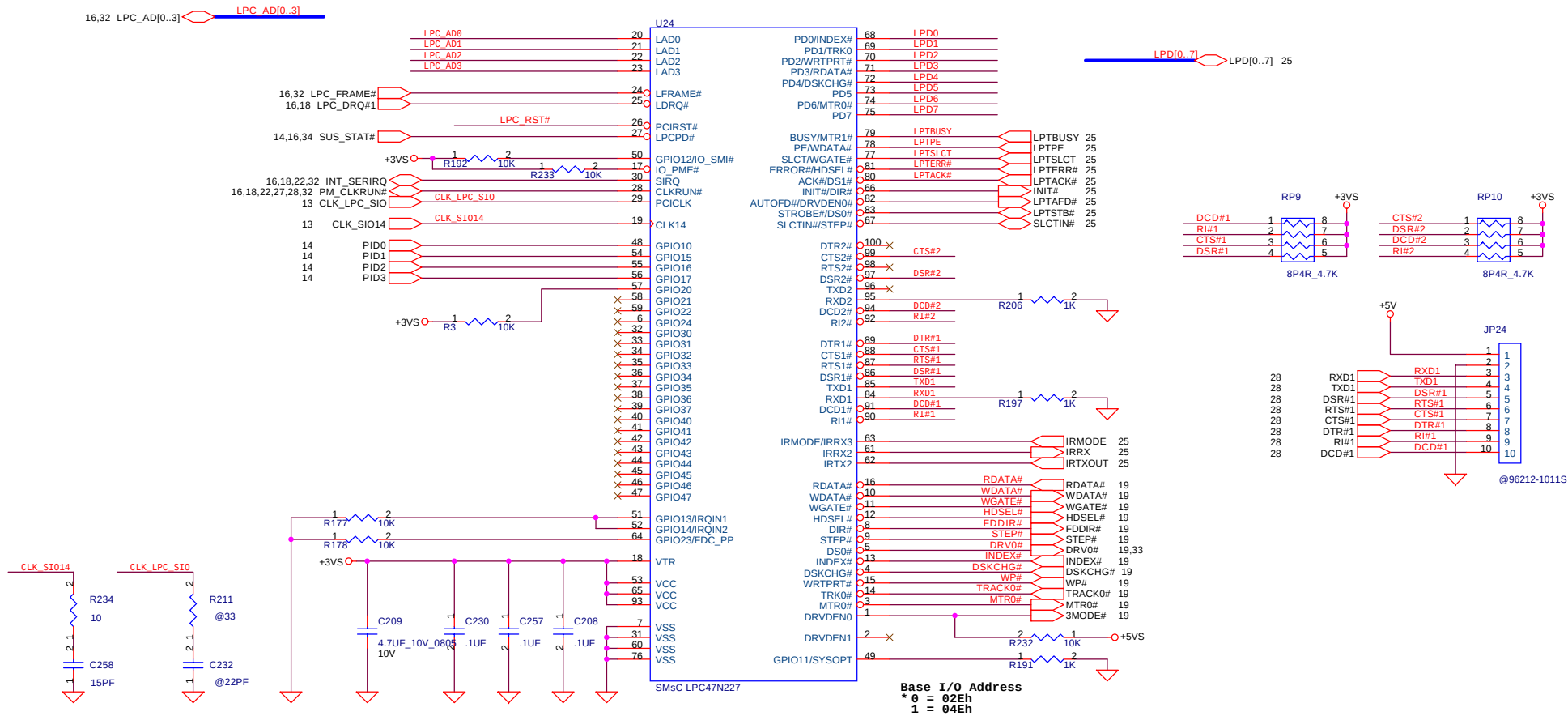
PCMCIA POWER CTRL.



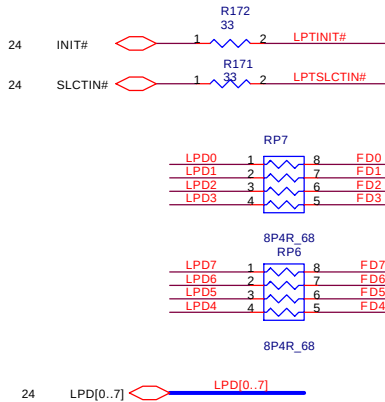
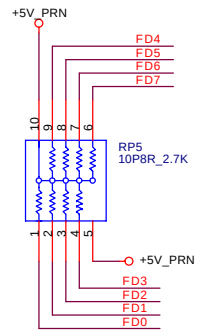
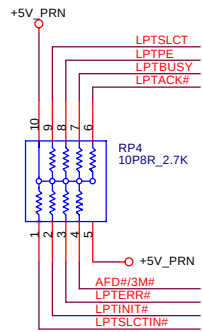
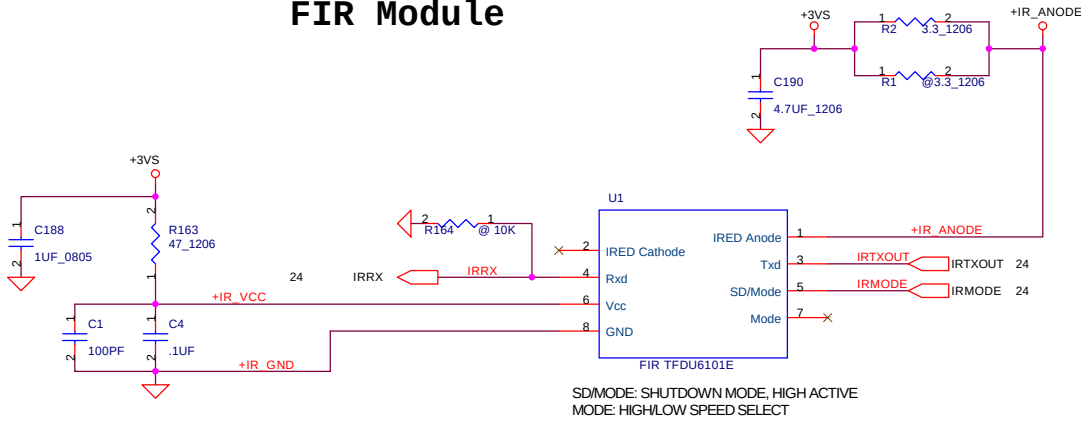
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SOCKET



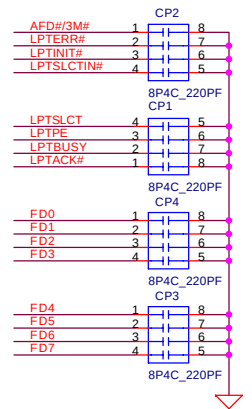
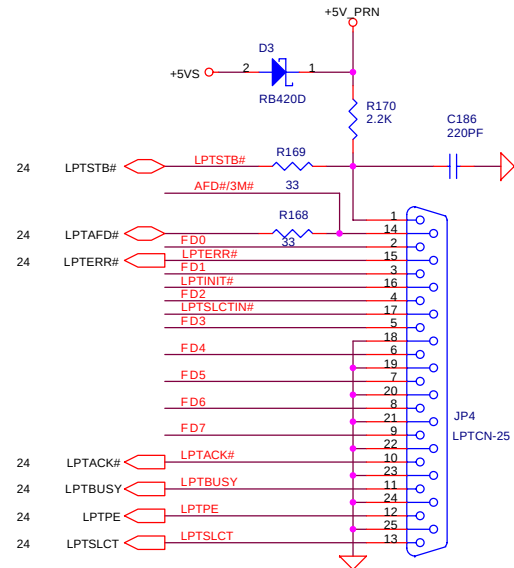
SUPER I/O SMsC FDC47N227



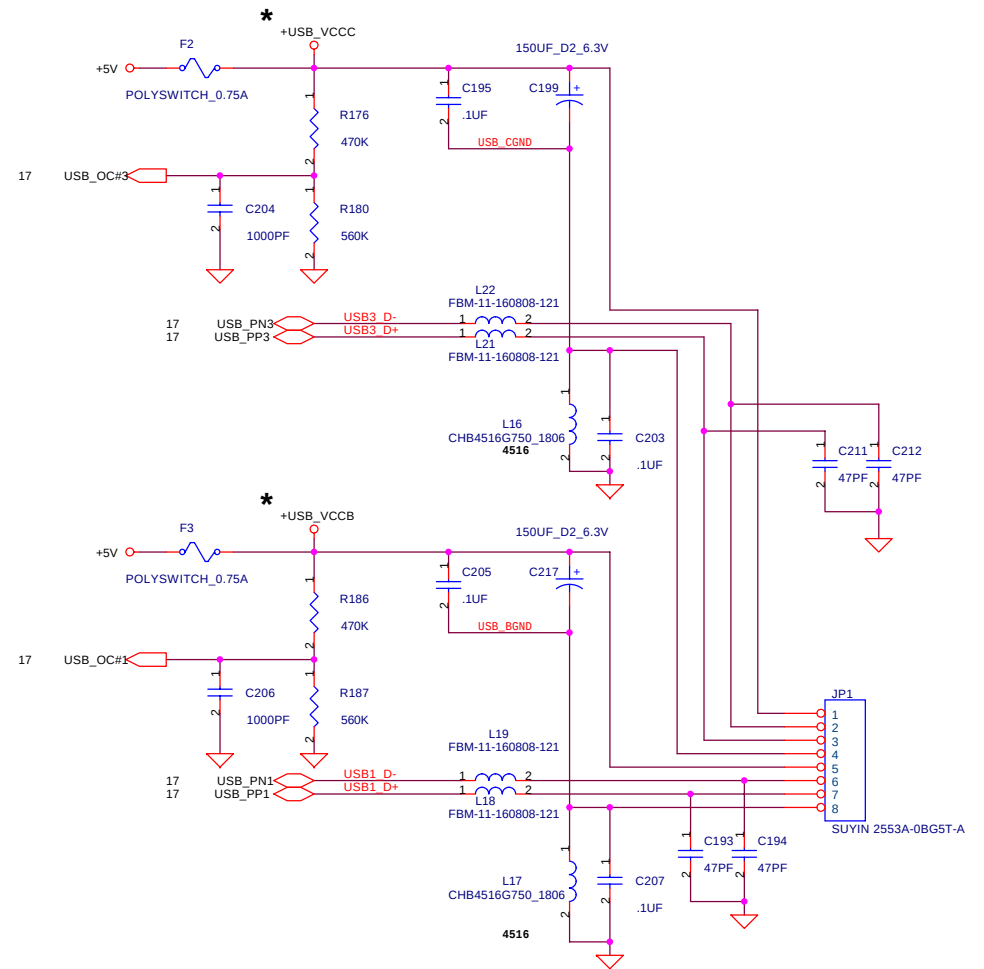
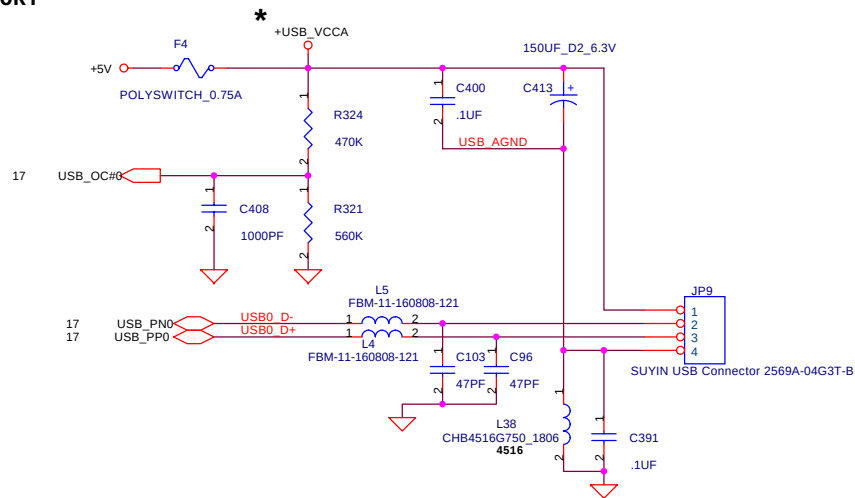
FIR Module



PARALLEL PORT



USB PORT

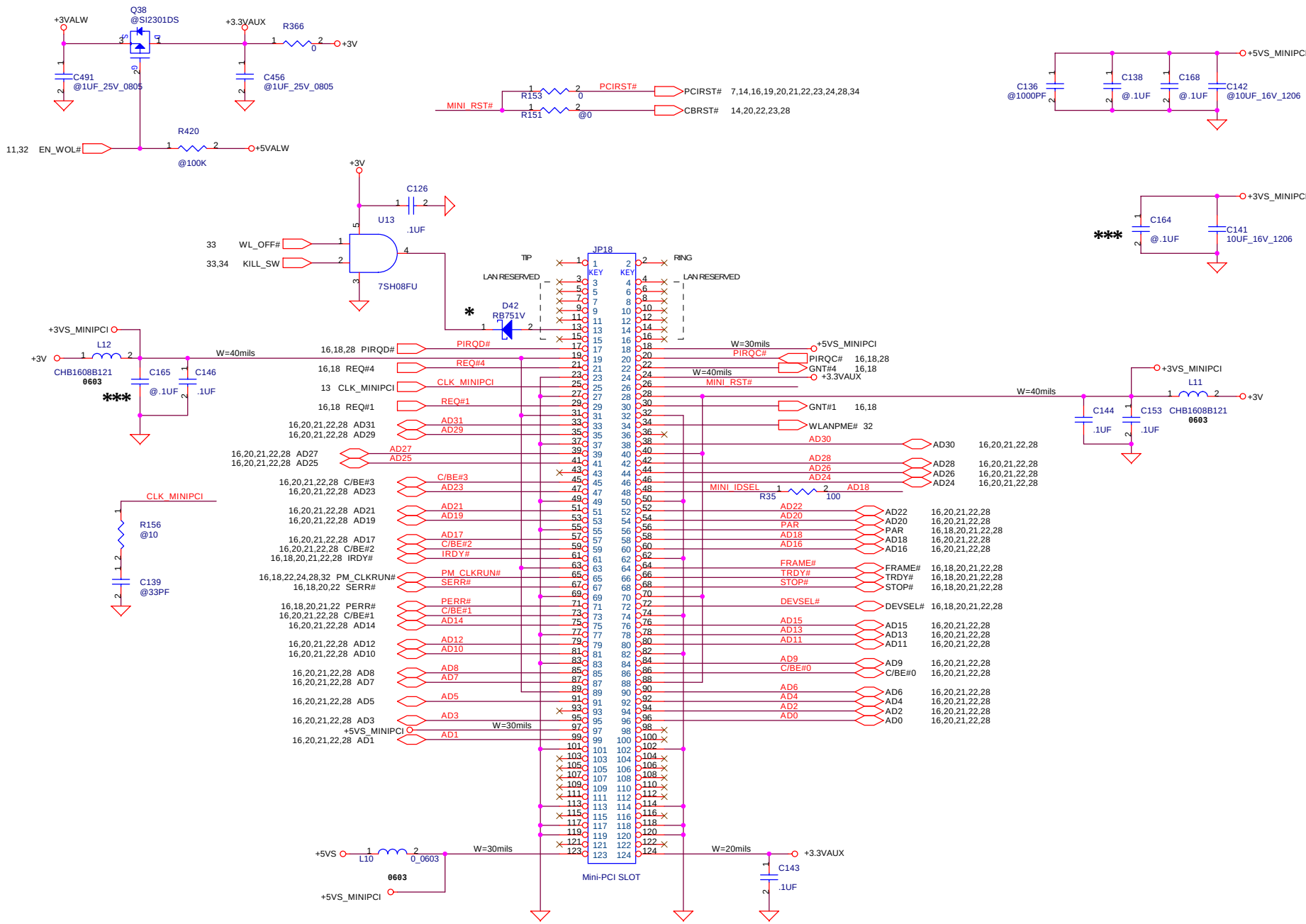


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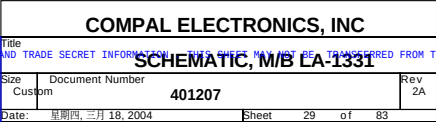
SCHEMATIC, M/B LA-1331

Size B	Document Number 401207	Rev 2A
Date:	星期四, 三月 18, 2004	Sheet 26 of 83

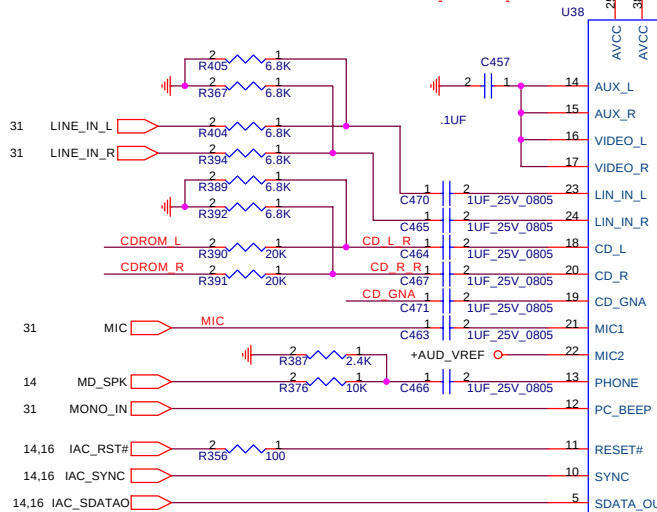
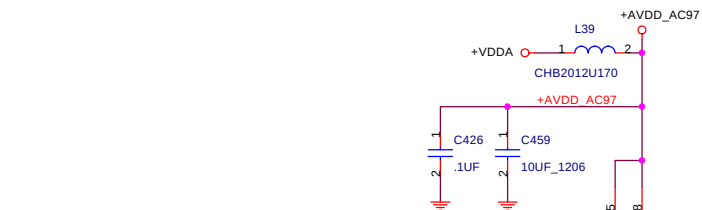
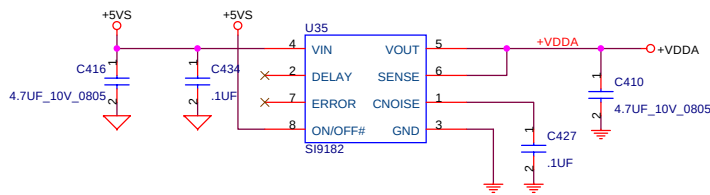


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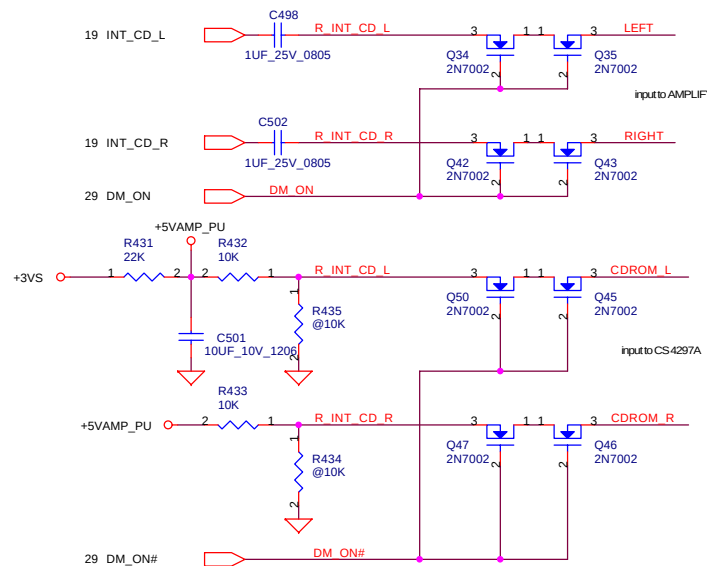
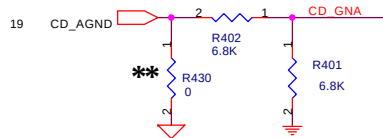
COMPAL ELECTRONICS, INC		
Title		
SCHEMATIC, M/B LA-1331		
Size B	Document Number	Rev 2A
	401207	
Date: 星期四, 三月 18, 2004	Sheet 27 of 83	



AC97 Codec



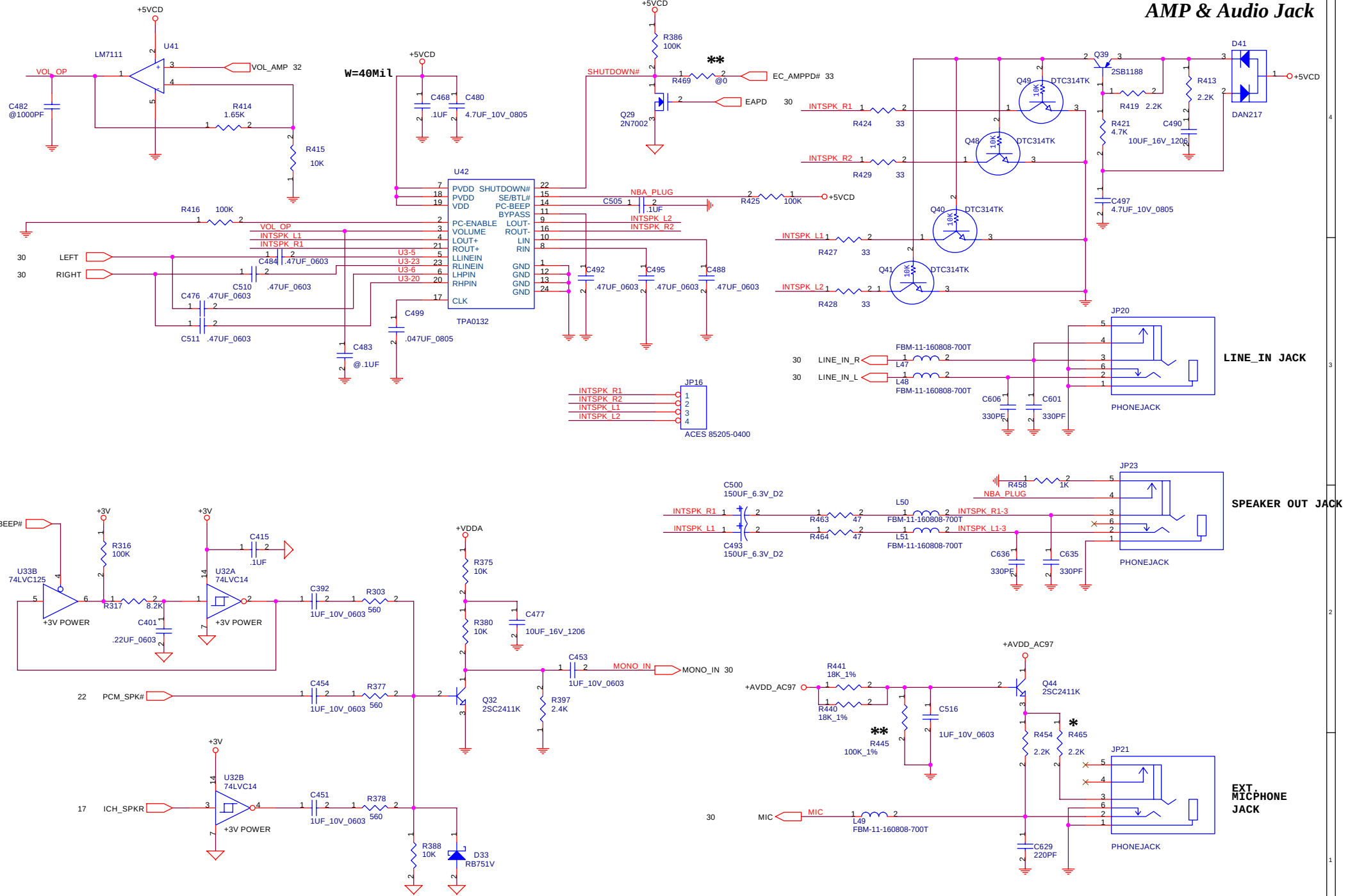
R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck



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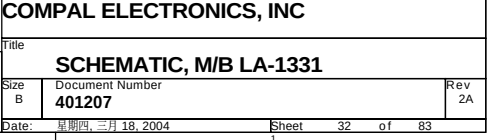
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Size B	Document Number	401207	Rev 2A
Date:	星期四, 三月 18, 2004	Sheet	30 of 83

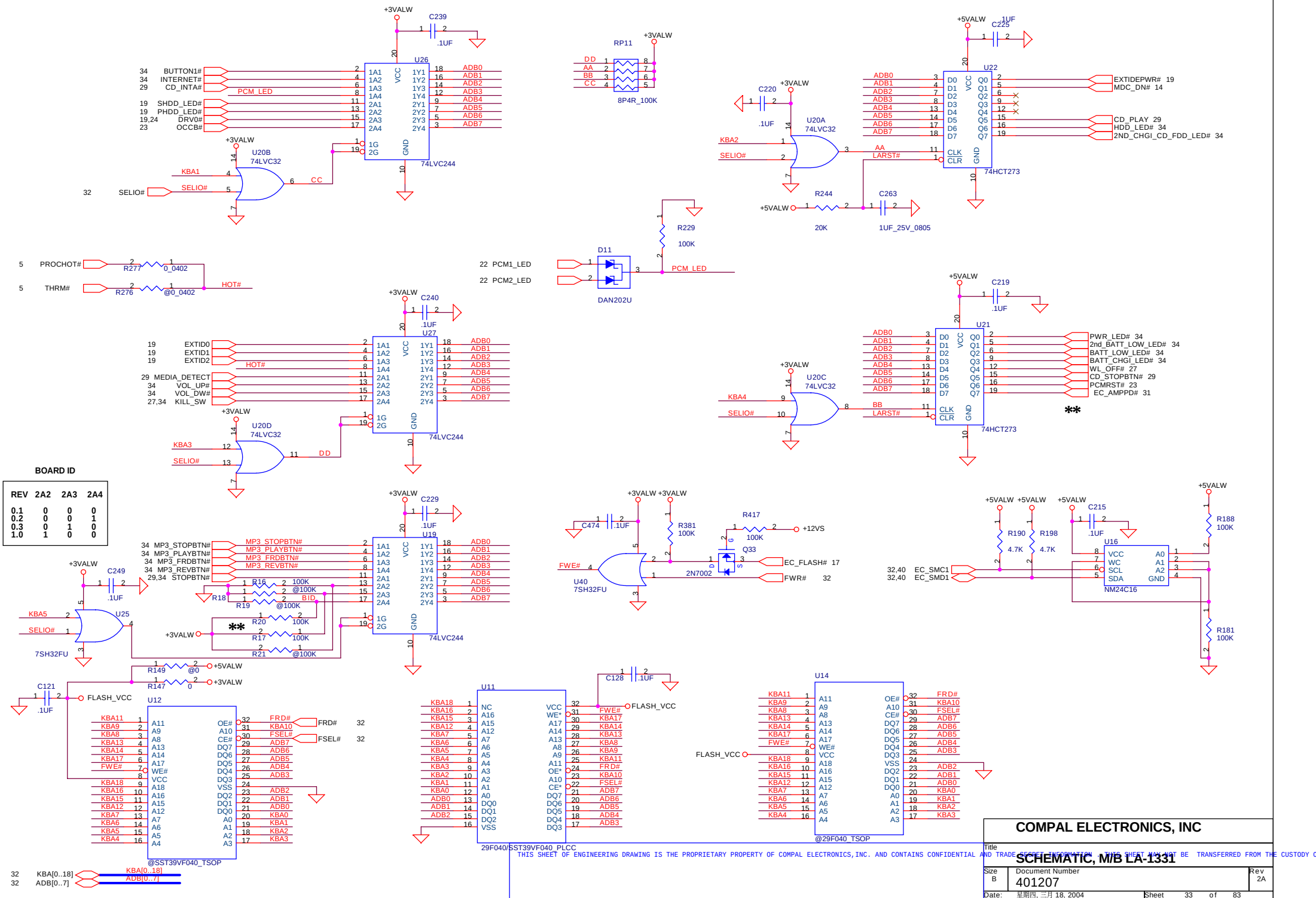
AMP & Audio Jack

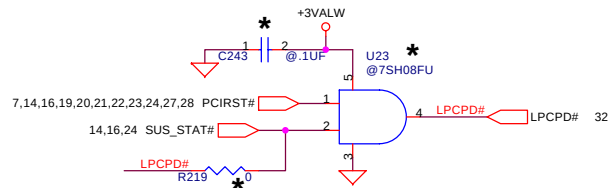
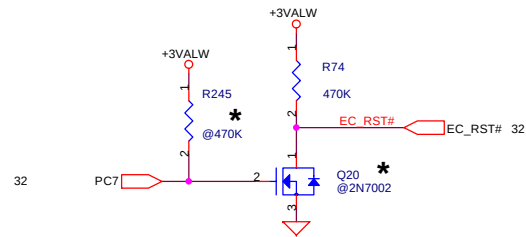


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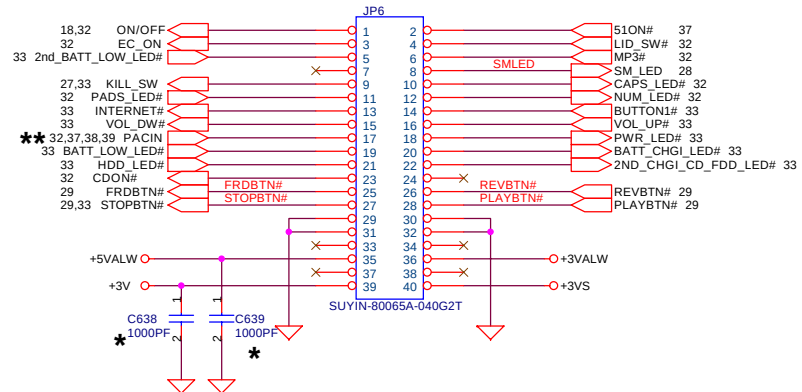
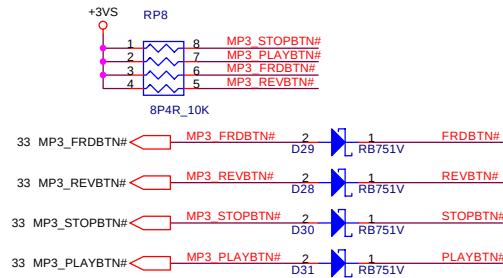
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Title			
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Size	Document Number	Rev	
B	401207	2A	
Date:	星期四, 三月 18, 2004	Sheet	31 of 83



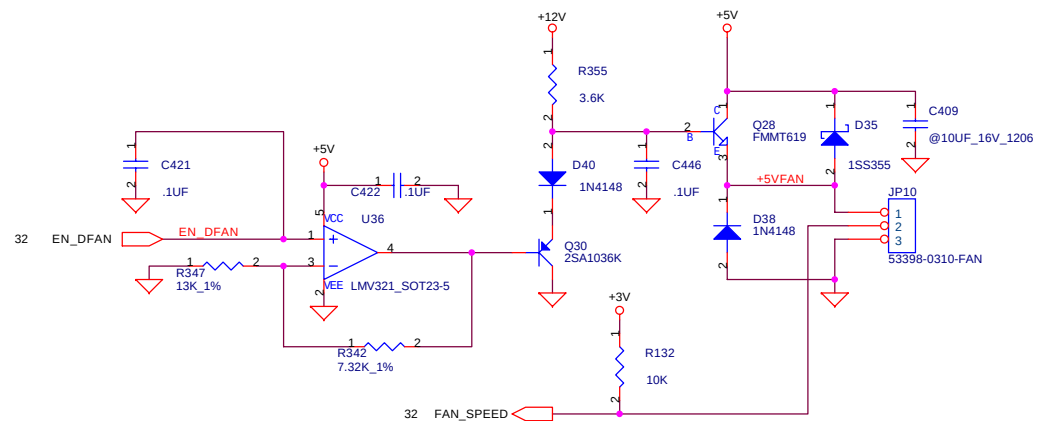




For PC87591 REV 0.A Only



FAN CONN.



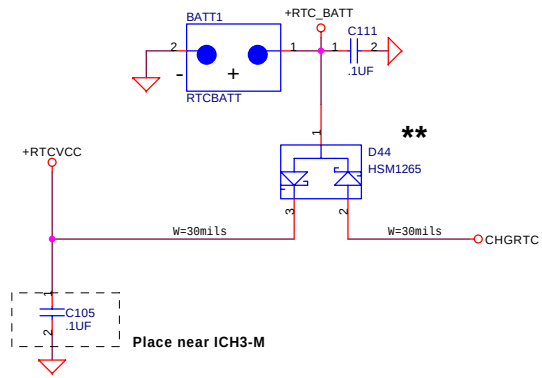
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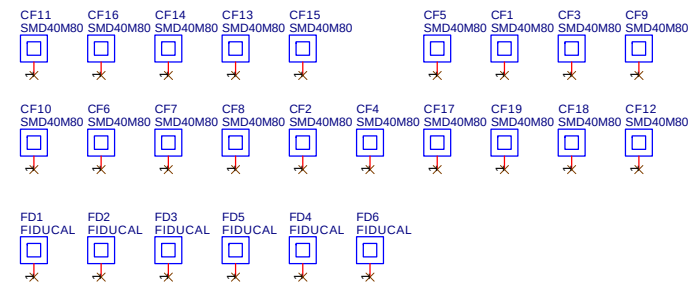
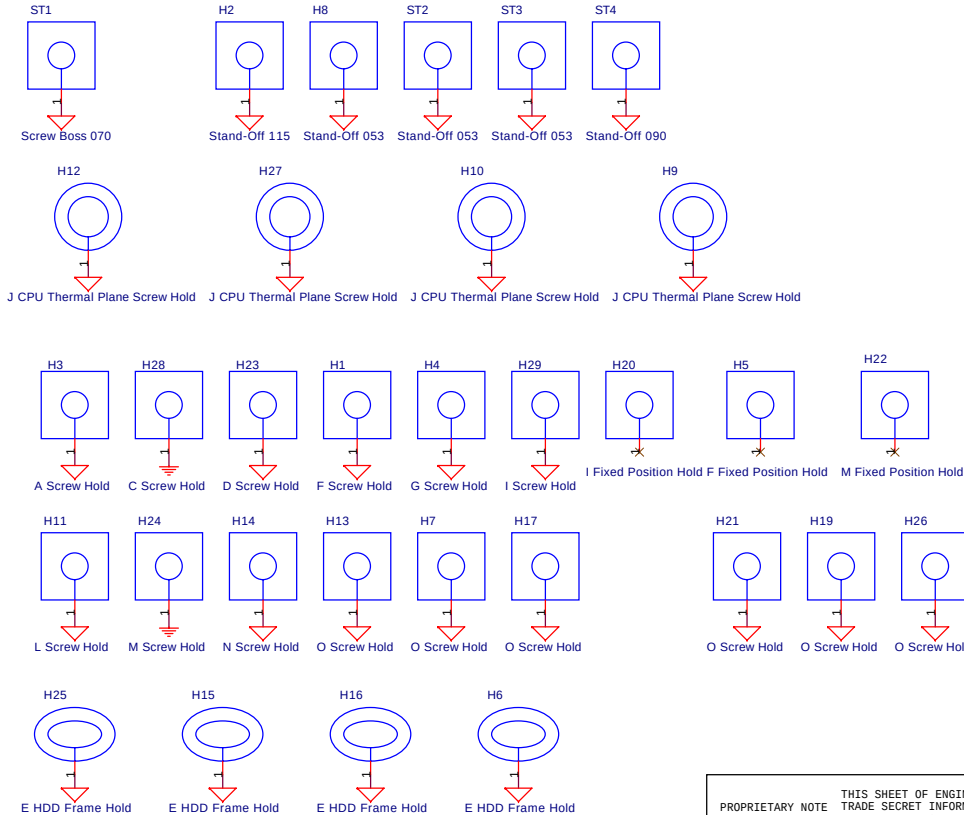
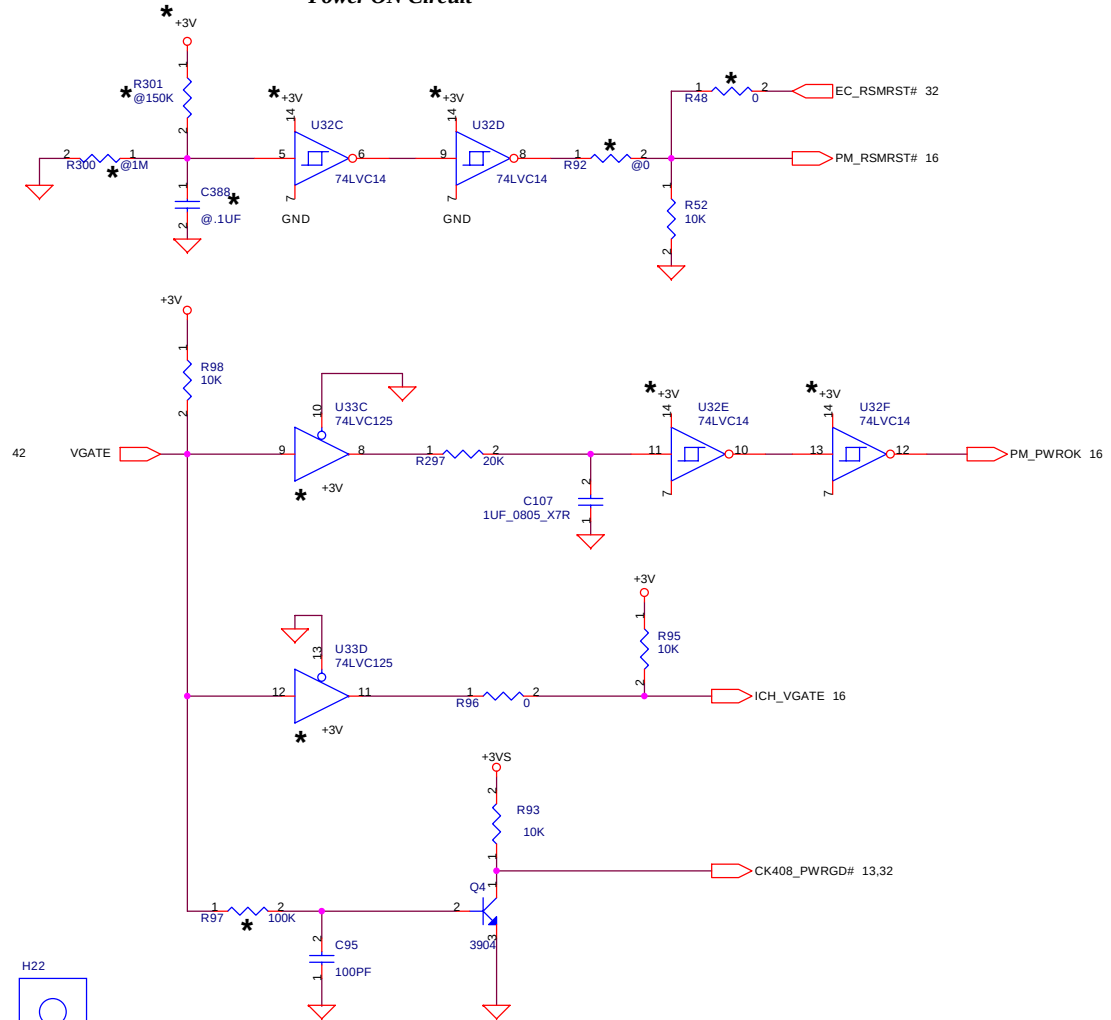
SCHMATIC, M/B LA-1331

Size	Document Number	Rev
B	401207	2A
Date:	星期四, 三月 18, 2004	Sheet 34 of 83

RTC Batt. Connector



Power ON Circuit



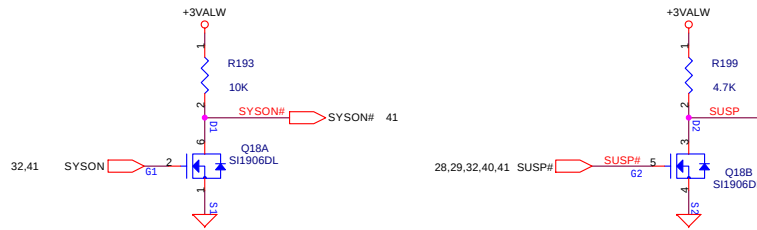
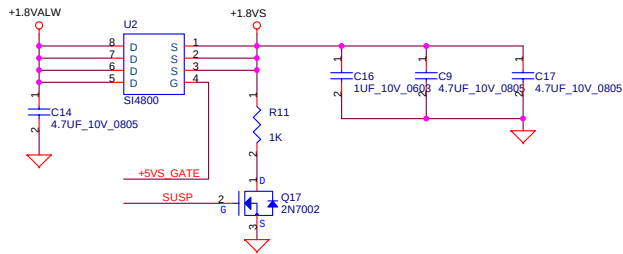
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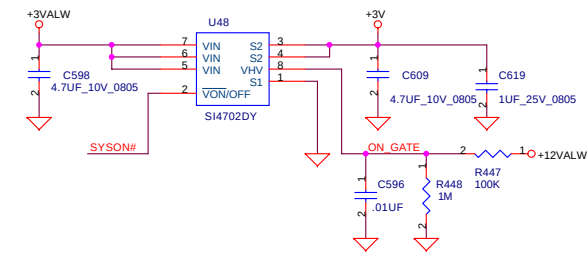
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Title		SCHEMATIC, M/B LA-1331	
Size	Custom	Document Number	401207
Date:	星期四, 三月 18, 2004	Sheet	35 of 83
		Rev	2A

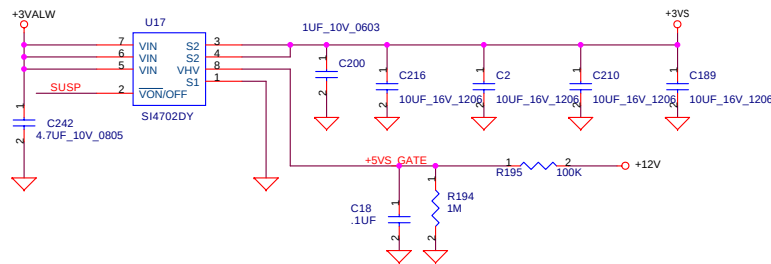
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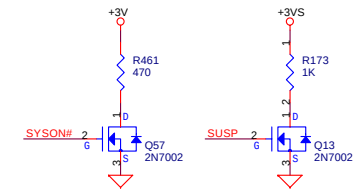
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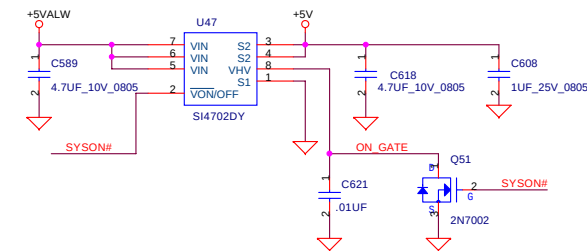
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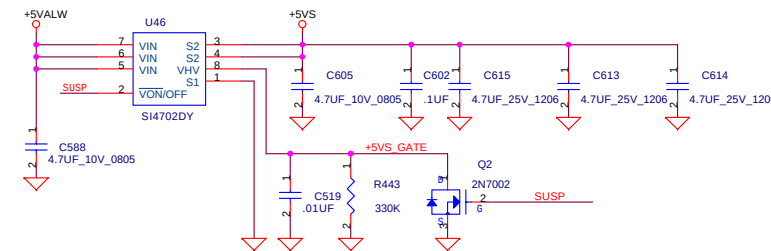
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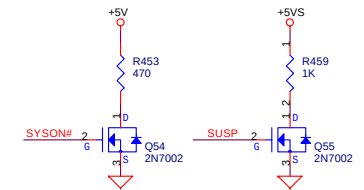
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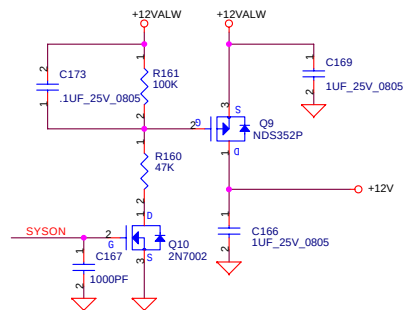
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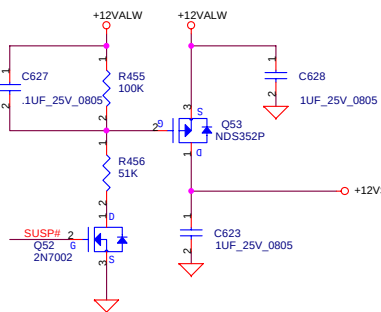
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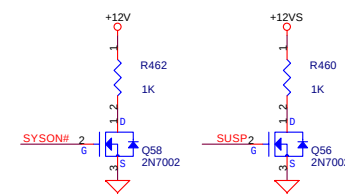
+12VALW To +12V Transfer



+12VALW To +12VS Transfer



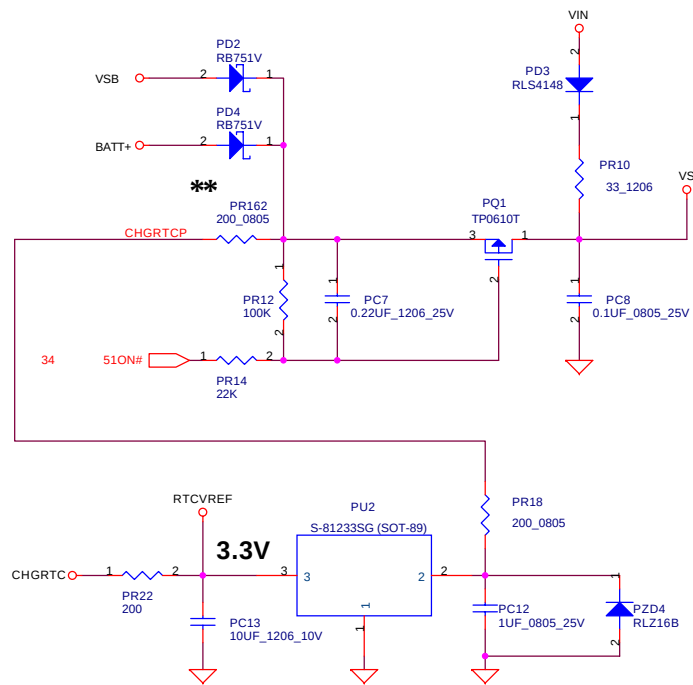
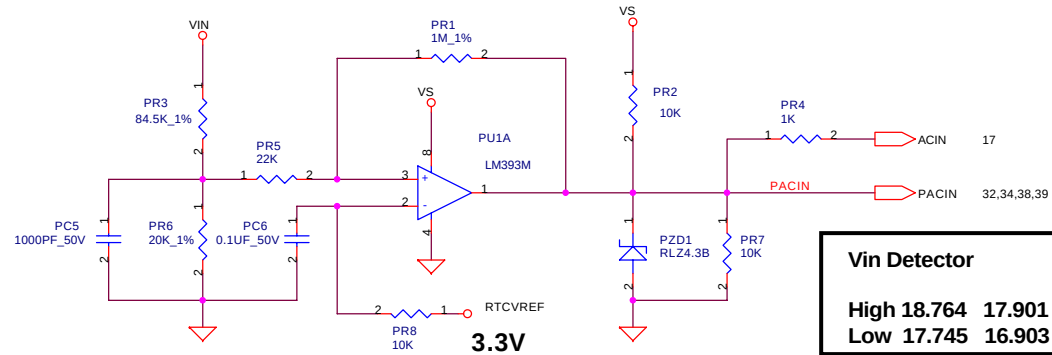
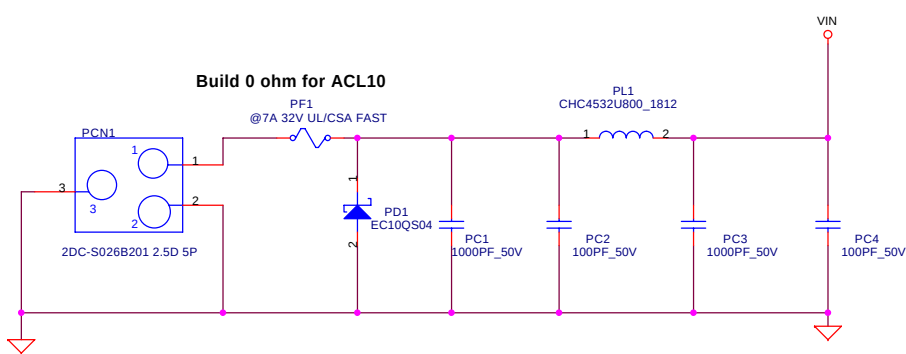
+12V & +12VS Discharge



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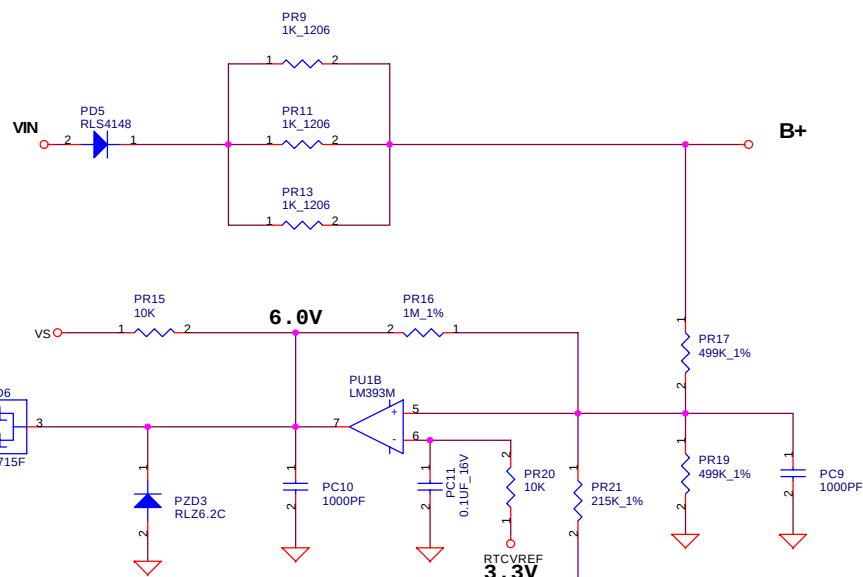
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Title			SCHEMATIC, M/B LA-1331
Size	Document Number	Rev	
Custom	401207	2A	
Date:	星期三, 三月 18, 2004	Sheet	36 of 83



39,40 MAINPWON

38 ACON



+2.5VP (6A,240mils ,Via NO.= 12)

+1.5VSP (2A,80mils ,Via NO.= 4)

+1.8VALWP (3A,120mils ,Via NO.= 6)

+12VALWP (120mA,20mils ,Via NO.= 1)

+5VALWP (5A,200mils ,Via NO.= 10)

+3VALWP (5A,200mils ,Via NO.= 10)

+1.25VSP (3A,120mils ,Via NO.= 6)

+1.2VPP (300mA,40mils ,Via NO.= 2)

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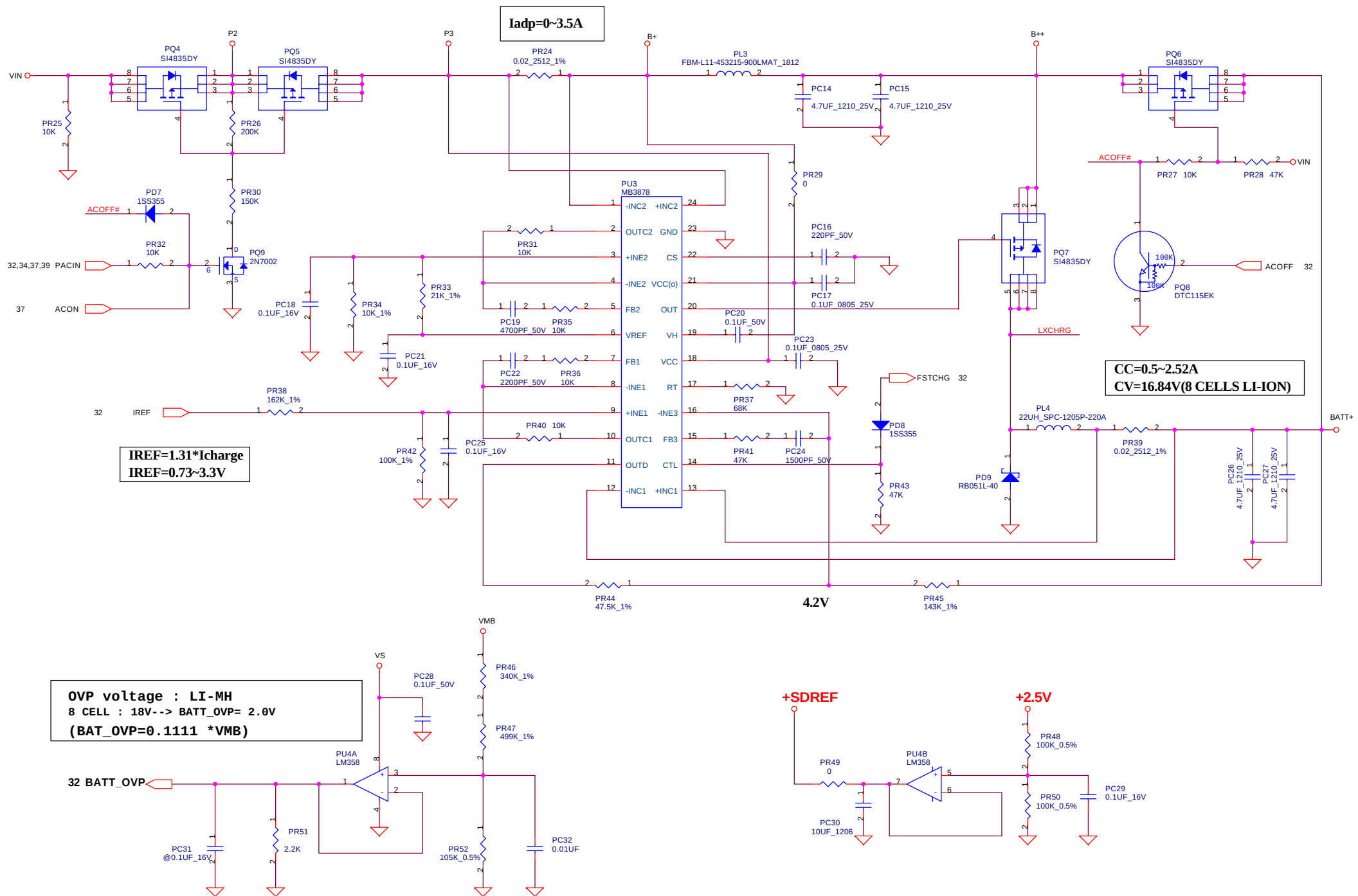
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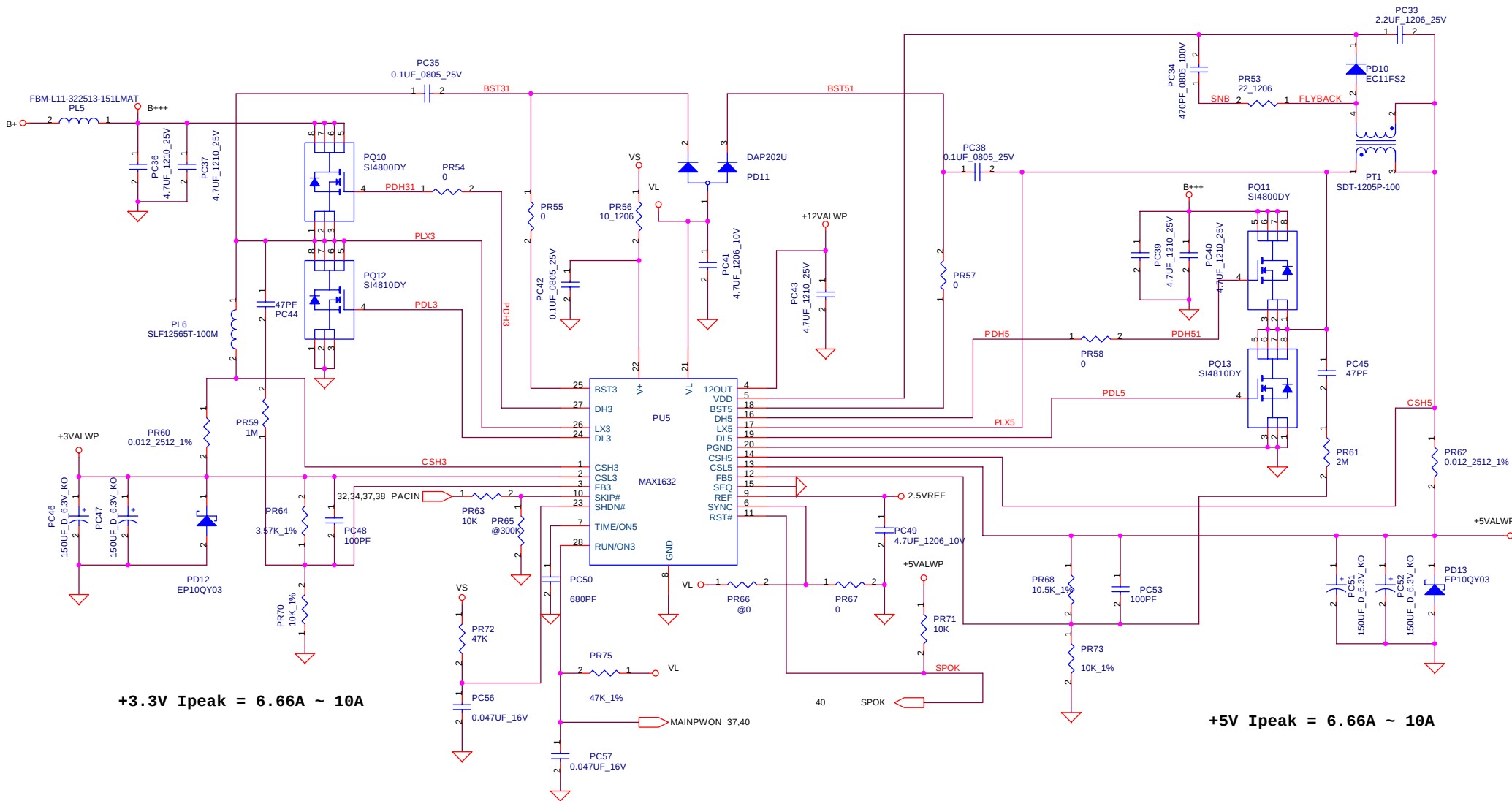
Sheet 37 of 83



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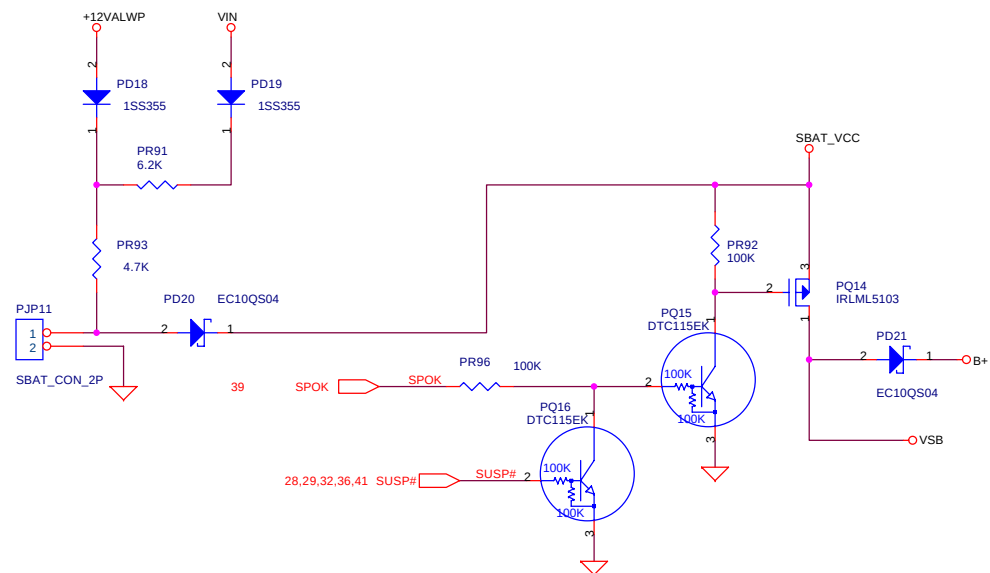
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Size	B	Document Number	401207
Date:	星期四, 三月 18, 2004	Sheet	38 of 83
Rev	2A		



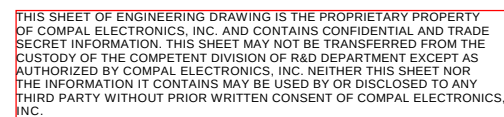
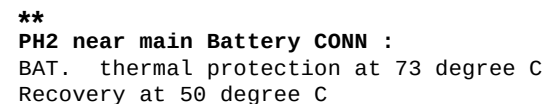
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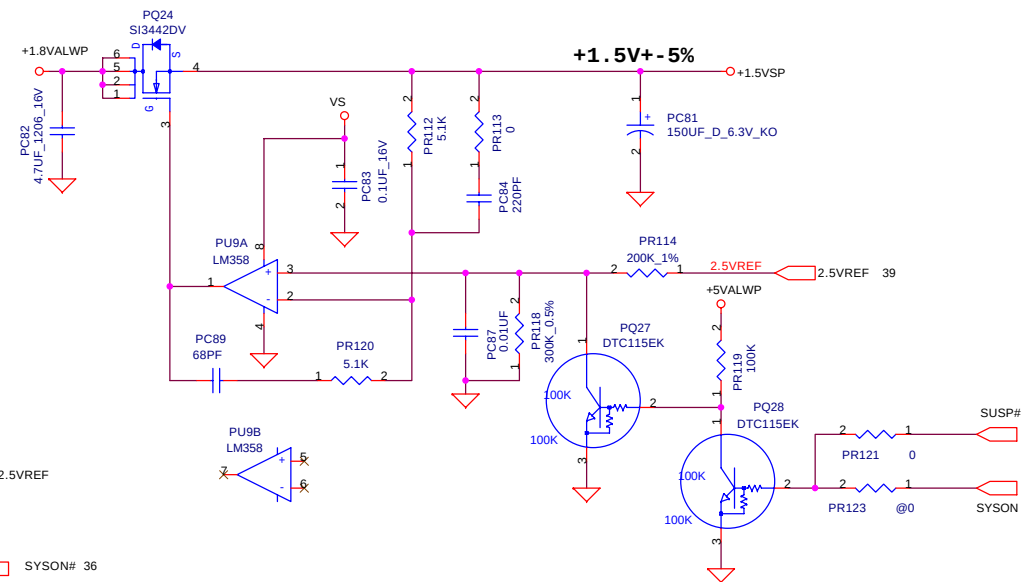
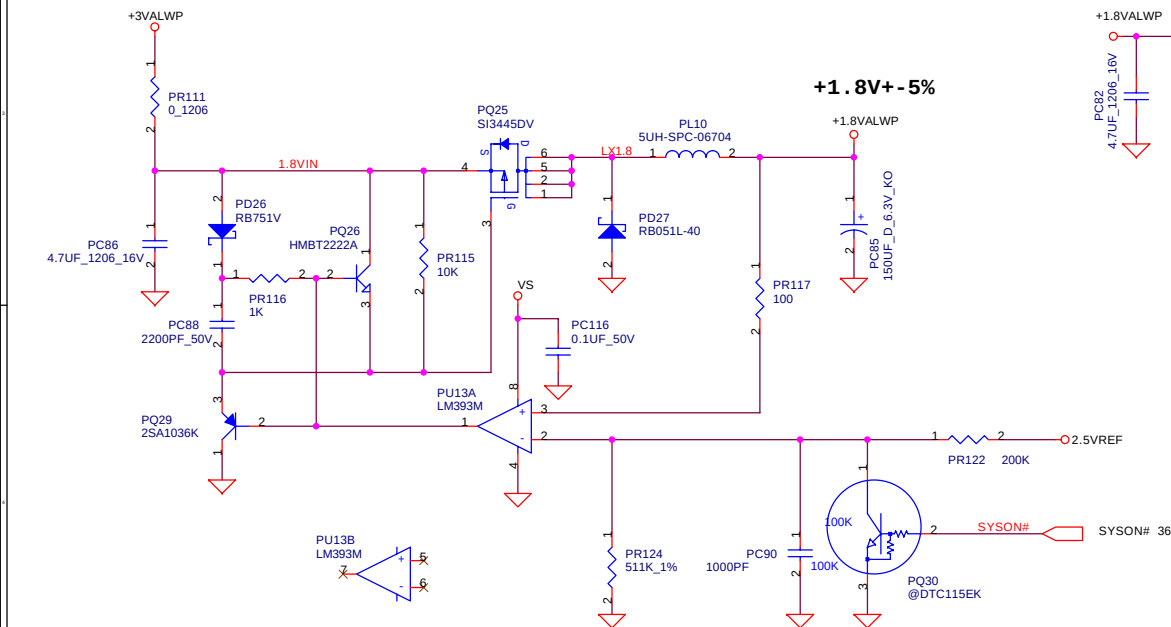
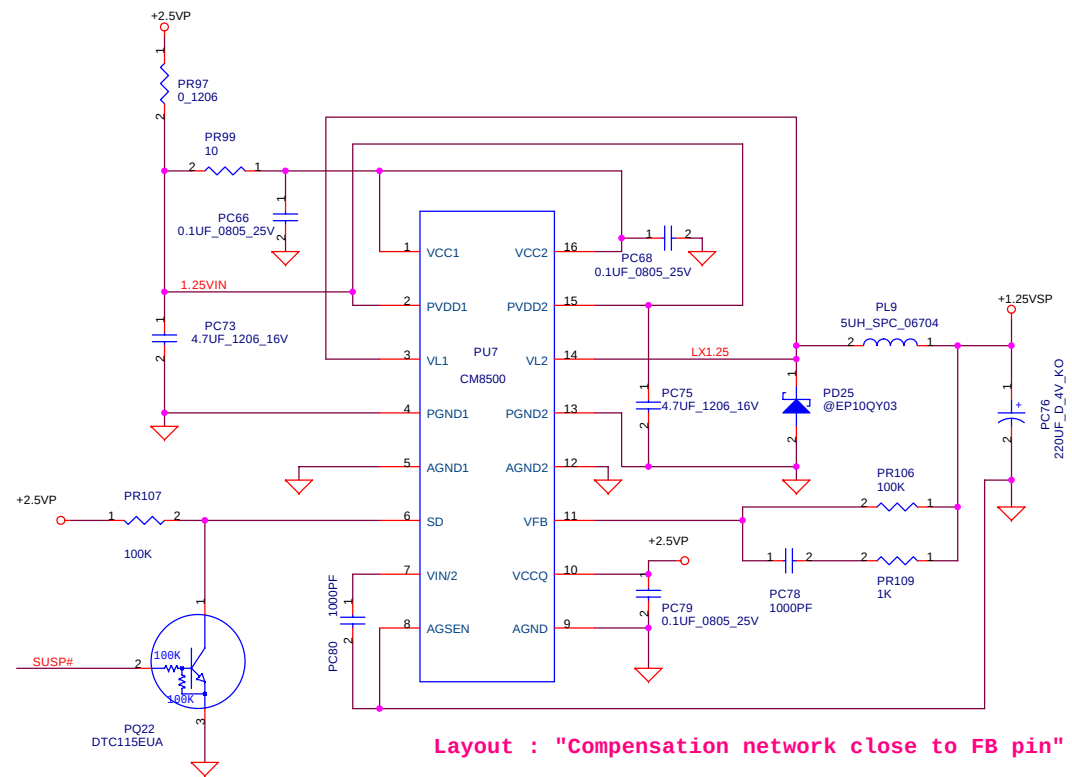
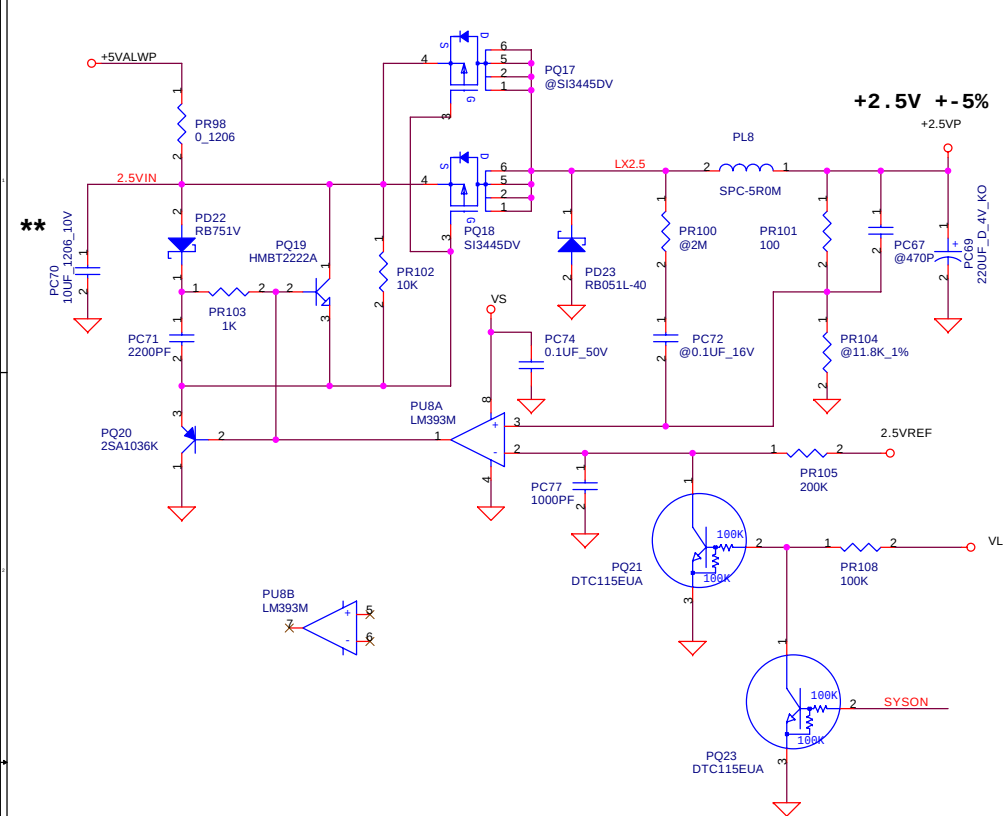
COMPAL ELECTRONICS, INC

Title		SCHEMATIC, M/B LA-1331	
Size	B	Document Number	401207
Date:	星期四, 三月 18, 2004	Sheet	39 of 83
Rev	2A		



PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C

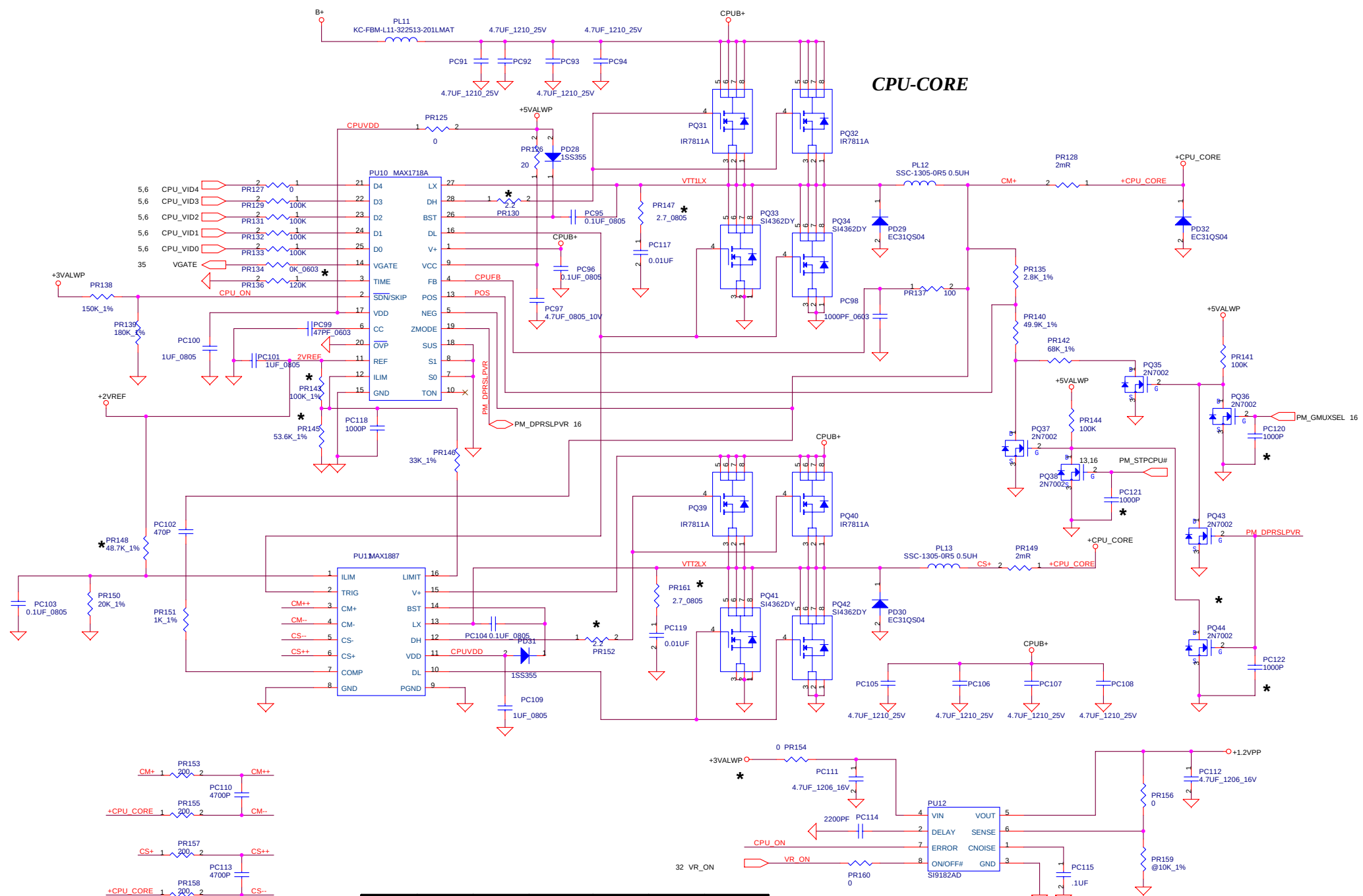




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Title		
SCHEMATIC, M/B LA-1331		
Size	Document Number	Rev
B	401207	2A
Date: 星期四, 三月 18, 2004		
Sheet 41 of 83		

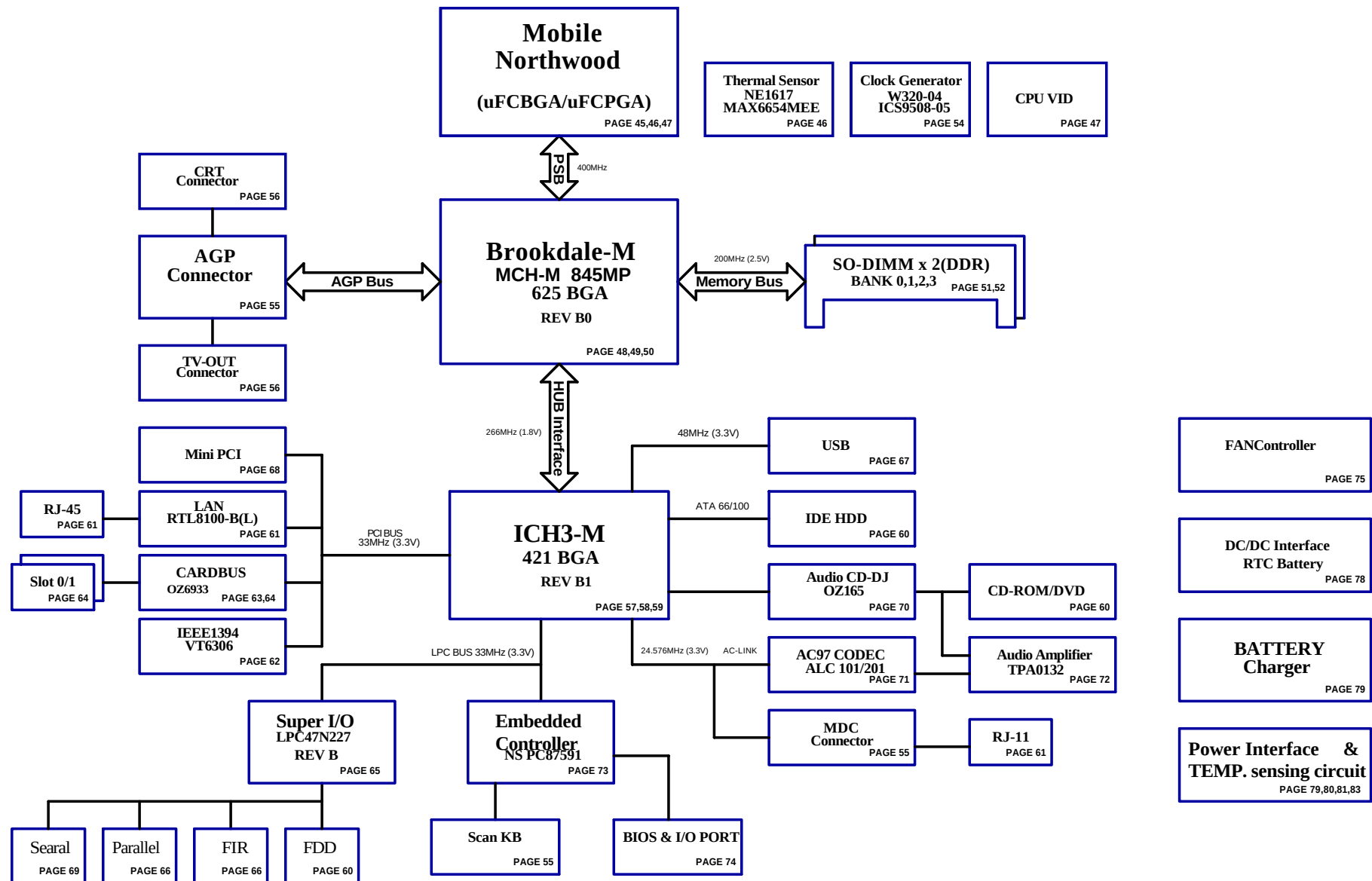


	GMUXSEL	CPUSTP#	DPRS_LPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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Size	Document Number	Rev	
B	401207	2A	
Date:	星期三, 三月 18, 2004	Sheet	42 of 83

ACL10 LA-1331 BLOCK DIAGRAM



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
1.2VP	1.2VP switched power rail for CPU VID	ON	OFF	OFF
+1.25VS	1.25VS power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V always power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON
+SDREF	+SDREF power	ON	ON	OFF

Note : "ON"" means that this power plane is "ON" only with AC power available, otherwise it is "OFF".

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
IEEE 1394	AD16	0	PIRQA
Mini-PCI	AD18	1/4	PIRQC/PIRQD
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
SM	AD22	-	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	MAX6654MEE	1001 110Xb
EEPROM(24C16/02)	1010 000Xb	OZ165	1011 0100b (B4h)
(24C04)	1011 000Xb	Smart Battery	0001 011Xb
		Docking	0011 011Xb
		DOT Board	XXXX XXXXb

EC SM Bus2 address

ICH3-M SM Bus address

Device	Address
Clock Generator W320-04 / ICS9508-05	1101 0000

DDR SODIMM SM Bus address

DDR SLOT	SA2	SA1	SA0
DDR SODIMM0 (REVERSE)	0	0	0
DDR SODIMM1 (NORMAL)	0	0	1

PIR

REV 0.1

Date	Page	Description
2001/12/29	7	Change R212,R214 & R213 to 8.2K ohm for Intel recommend
2001/12/29	14	Stuff R361=22 Ohm and no-stuff R360 for Data-IN1 of MDC module.
2001/12/29	15	Change L28 & L29 to 0 Ohm for EMI issue.
2001/12/29	16	Change R39 power-plane to +3VALW for Resume-well Power-plane(+3VALW)
2001/12/29	17	DEL C73, C87, C371 for EMI issue.
2001/12/29	17	Change L37 power-plane to +1.8VS for Intel recommend.
2001/12/29	17	Change R279 power-plane to +3VS for Intel recommend.
2001/12/29	17	Change U29 pinV22,U18 & P14 power-plane to +CPU_CORE for Intel recommend.
2001/12/29	17	Change R284 power-plane to +3VALW for Intel recommend.
2001/12/29	18	Change "SMB_ALERT#" power-plane to +3VALW for "RESUME-WELL" power-plane(+3VLAW).
2001/12/29	18	Exchang D13,D14,D16,D17,D18 and R28,R34,R30,R29 to RP135,R466,R468 for cost-down.
2001/12/29	20	Add D43 for leakage.
2001/12/29	21	Exchang L42 to L52,L53, L54, L55 for ME limitation.
2001/12/29	27	Add D42 for leakage.
2001/12/29	31	Add R465 for PC99 Spec.
2001/12/29	34	Add C368, C369 for EMI solution.
2001/12/29	35	EC control "EC_RSMRST#". ->DEL R92, Stuff R48.
2001/12/29	35	Change R97 to 100K for "VGATE" of Max1718A issue.-> Change PR134= 0 Ohm.
2002/01/07	39	Change PR68 from 10k_1% to 10.5k_1%.(increase 5valvp to 5.125v).
2002/01/07	40	Change PR81 from 2.15k_1% to 1.87k_1%.(CPU thermal OTP from 83+-3C to 85+-3C).
2002/01/07	42	Add PR147, PR161 to 2.7_0805. for EMI requirement.
2002/01/07	42	Add PC120, PC121, PC122 to 1000pf. for ESD.
2002/01/07	42	Add PQ44 to 2N7002 for CPU SPEED STEP.
2002/01/07	42	Change PR130, PR152 from 0 to 2.2. for EMI requirement.
2002/01/07	42	Change PR143 from 53.6k_1% to 100k_1%. for CPU OCP.
2002/01/07	42	Change PR145 from 100k_1% to 53.6k_1%. for CPU OCP.
2002/01/07	42	Change PR148 from 30k_1% to 48.7k_1%. for CPU OCP.
2002/01/07	42	Change PU12 VIN from +2.5VP to +3VALWP.

REV 0.2

Date	Page	Description
2002/01/11	40	Change PH1 and PH2 design by high active for AC-IN issue.

REV 0.3

Date	Page	Description
None		

REV 1.0

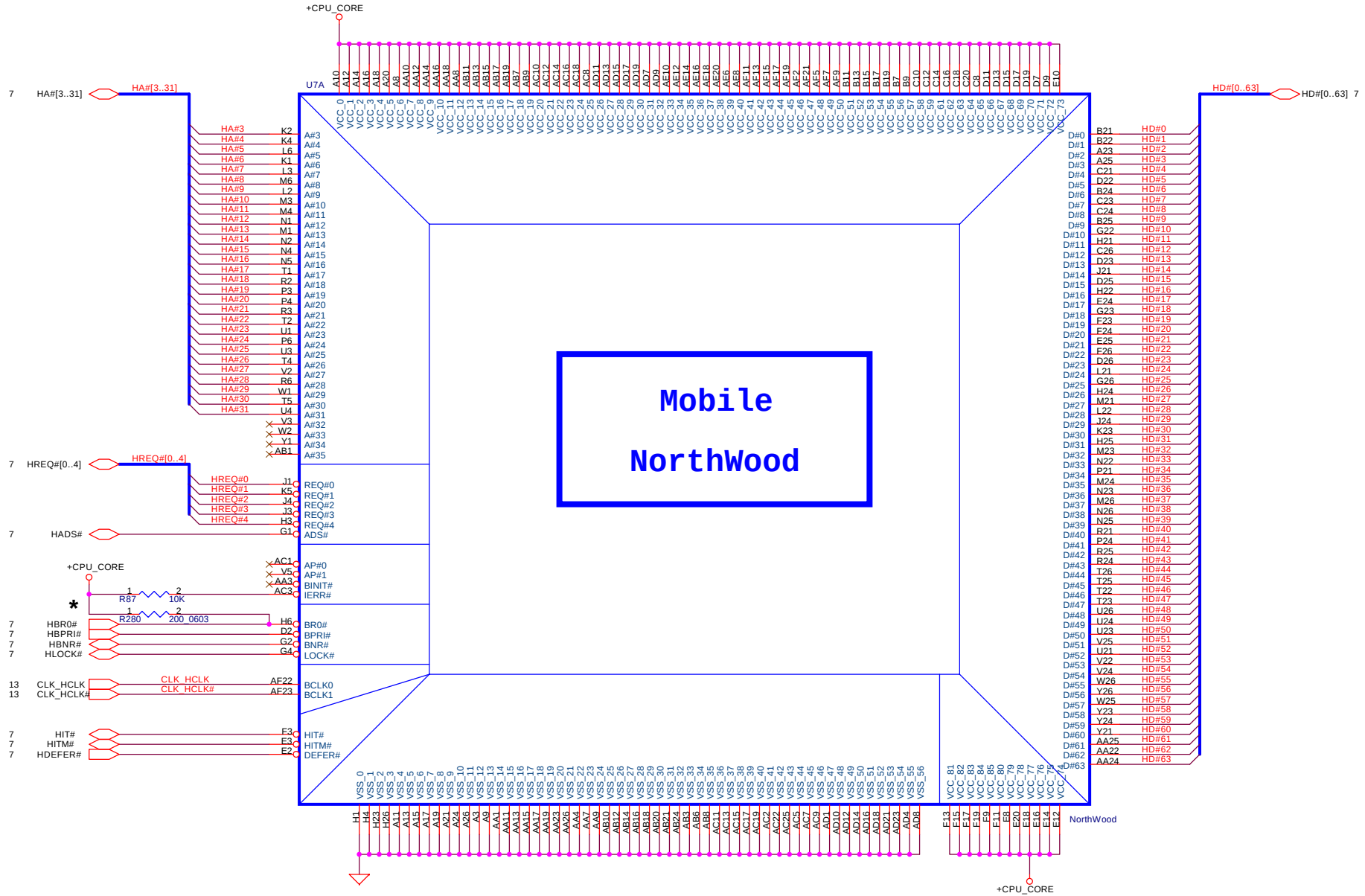
Date	Page
None	

REV 2.0

Date	Page	
2002/04/10	20	GCR: (For LAN Issue) <1>Isolation U18 pin6 for Realtek application notice. <2>Change R204 from 5.9K+-1% to 5.6K +-1%. <3>Change L23 from 4.7UH to 0 ohm.

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Title			
SCHEMATIC, MB LA-1331			
Size	Document Number		Rev
Custom	401207		2A
Date:	星期四, 三月 18, 2004		Sheet 44 of 83

Mobile NorthWood



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Title		SCHEMATIC, M/B LA-1331	
Size	Custom	Document Number	401207
Date:	星期三, 三月 18, 2004	Sheet	45 of 83
Rev	2A		

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Place close to CPU, Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

Three circuit diagrams showing the connection of capacitors to the +CPU_CORE supply rail. Each capacitor is connected in parallel to the supply rail and ground. The capacitors are labeled with their values: 10UF_6.3V_1206_X5R.

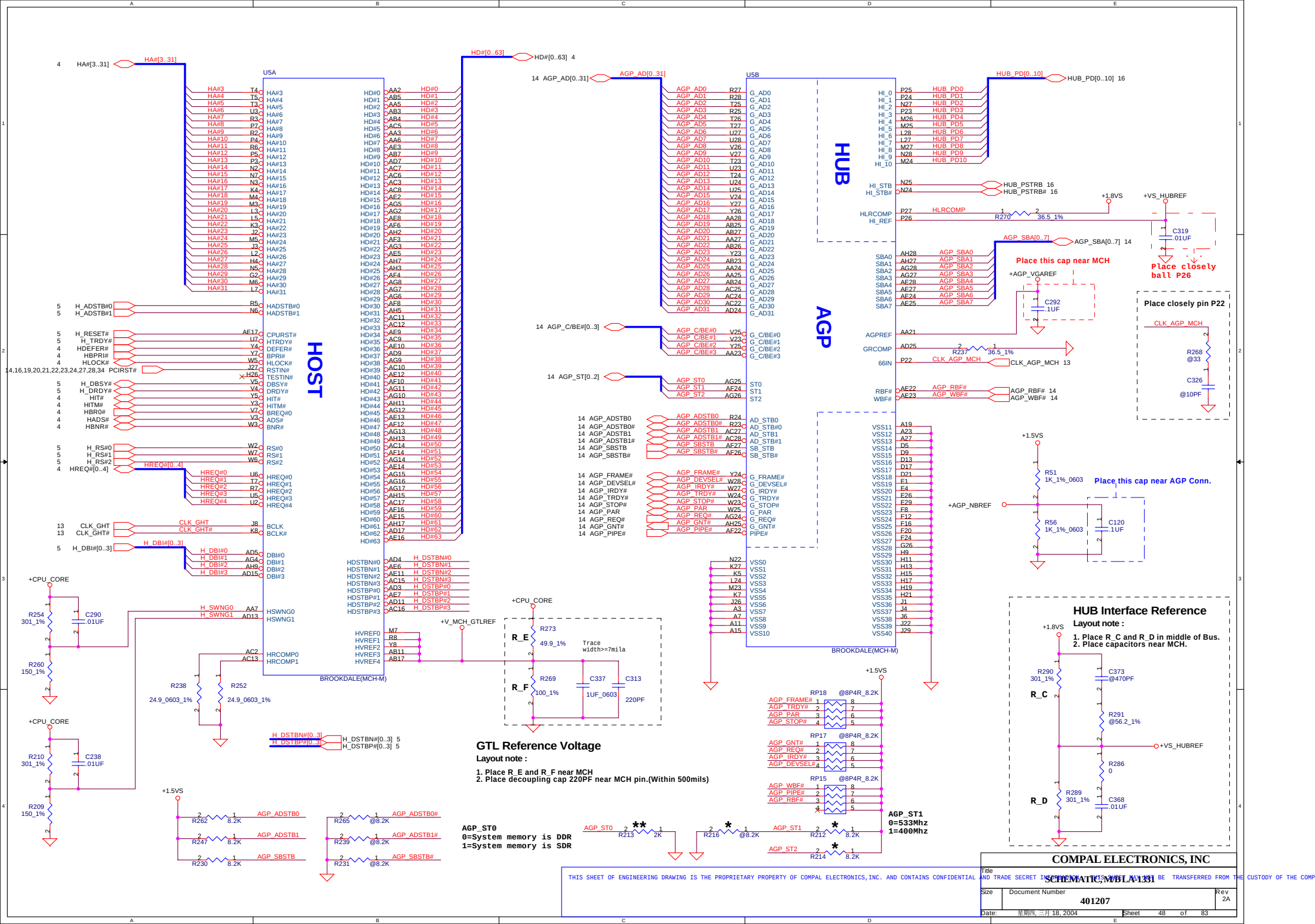
- Diagram 1:** Shows capacitors C24, C26, C30, C45, and C52 connected to the +CPU_CORE supply rail.
- Diagram 2:** Shows capacitors C62, C65, C22, C302, and C311 connected to the +CPU_CORE supply rail.
- Diagram 3:** Shows capacitors C320, C329, C344, and C351 connected to the +CPU_CORE supply rail.

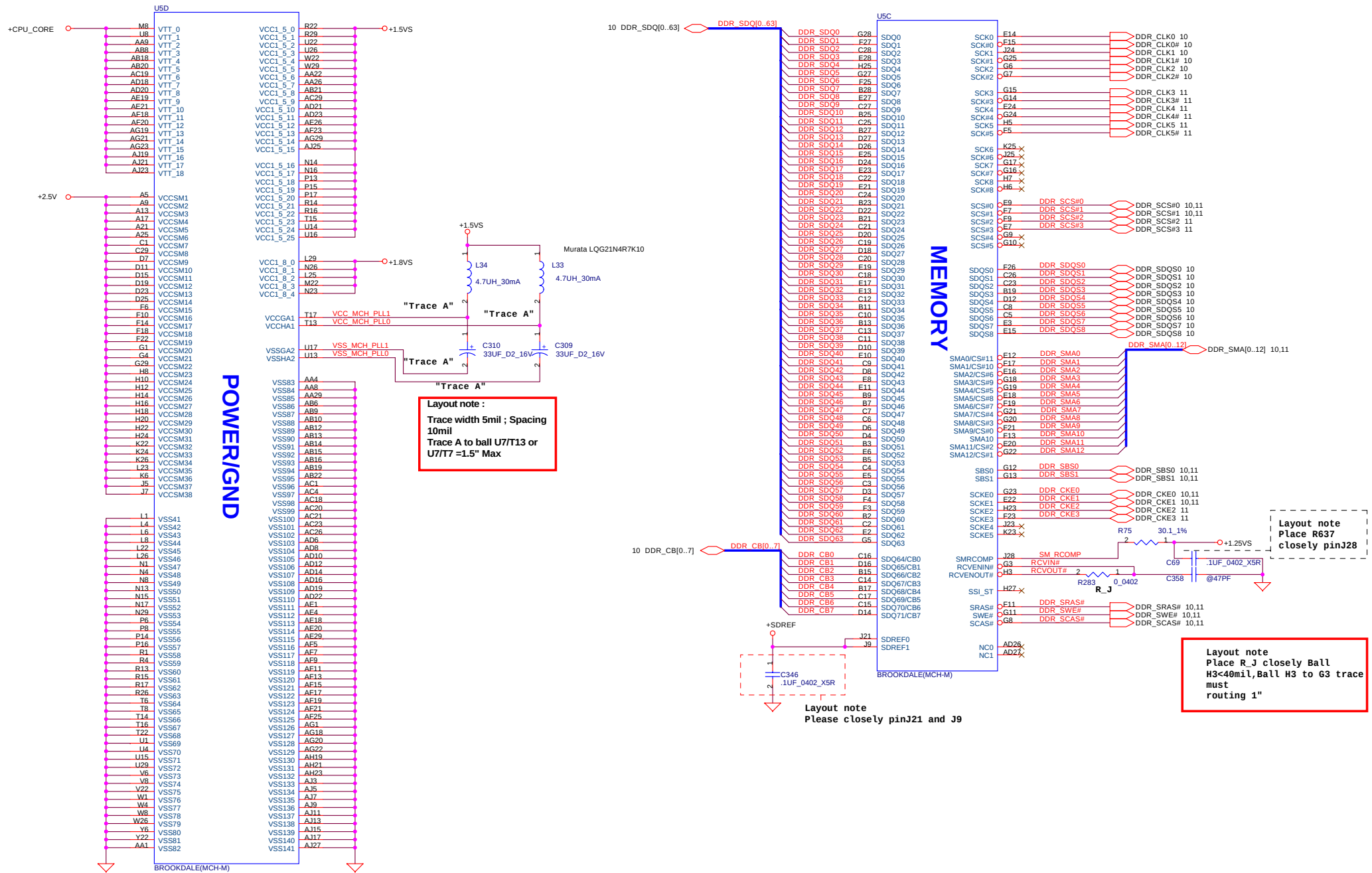
Place close to CPU power and ground pin as possible (<1inch)

Three circuit diagrams illustrating decoupling capacitor placement for different power planes:

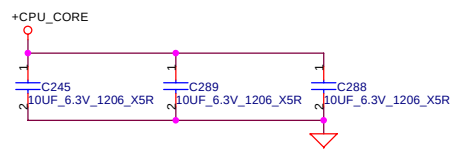
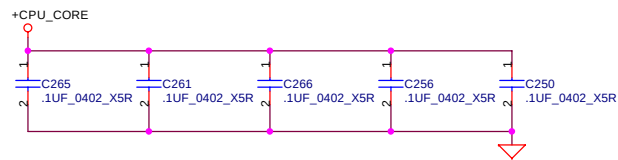
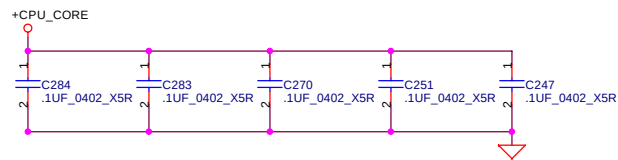
- Top Diagram:** Shows a series of capacitors (C380, C381, C382, C383, C384) connected to a +CPU_CORE plane. Each capacitor is labeled with its value (220UF_D2_4V_25m) and a reference designator (@220UF_D2_4V_25m).
- Middle Diagram:** Shows a series of capacitors (C385, C387, C388, C386, C390) connected to a +CPU_CORE plane. Each capacitor is labeled with its value (220UF_D2_4V_25m) and a reference designator (@220UF_D2_4V_25m).
- Bottom Diagram:** Shows a series of capacitors (C297, C296, C295, C294, C293, C338, C339, C340, C341, C342) connected to a +CPU_CORE plane. Each capacitor is labeled with its value (22UF_X7R) and a reference designator (@22UF_X7R).

5,42 CPU_VR_VID0 5,42 CPU_VID0 5,42
 5,42 CPU_VR_VID1 5,42 CPU_VID1 5,42
 5,42 CPU_VR_VID2 5,42 CPU_VID2 5,42
 5,42 CPU_VR_VID3 5,42 CPU_VID3 5,42
 5,42 CPU_VR_VID4 5,42 CPU_VID4 5,42

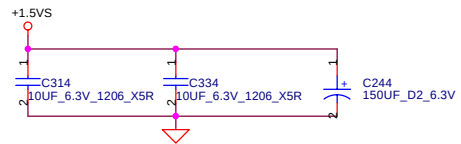
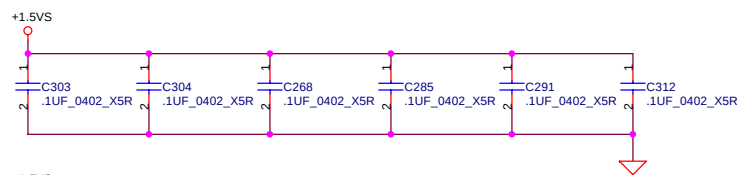




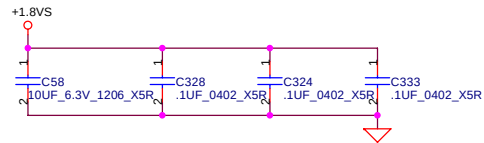
Layout note : Processor system bus
Distribute as close as possible
to MCH Processor Quadrant.(between VTTFSB and VSS pin)



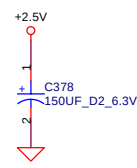
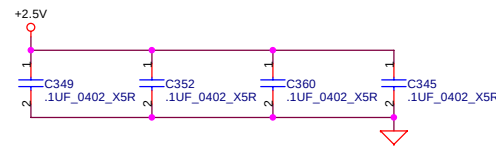
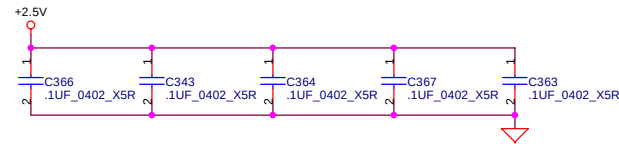
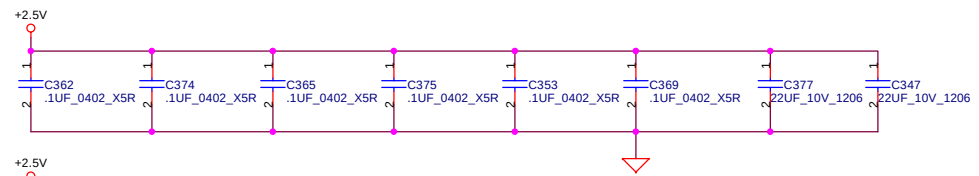
Layout note : AGP/CORE
Distribute as close as possible
to MCH Processor Quadrant.(between VCCAGP/VCCCORE
and VSS pin)

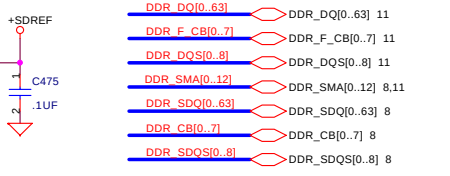
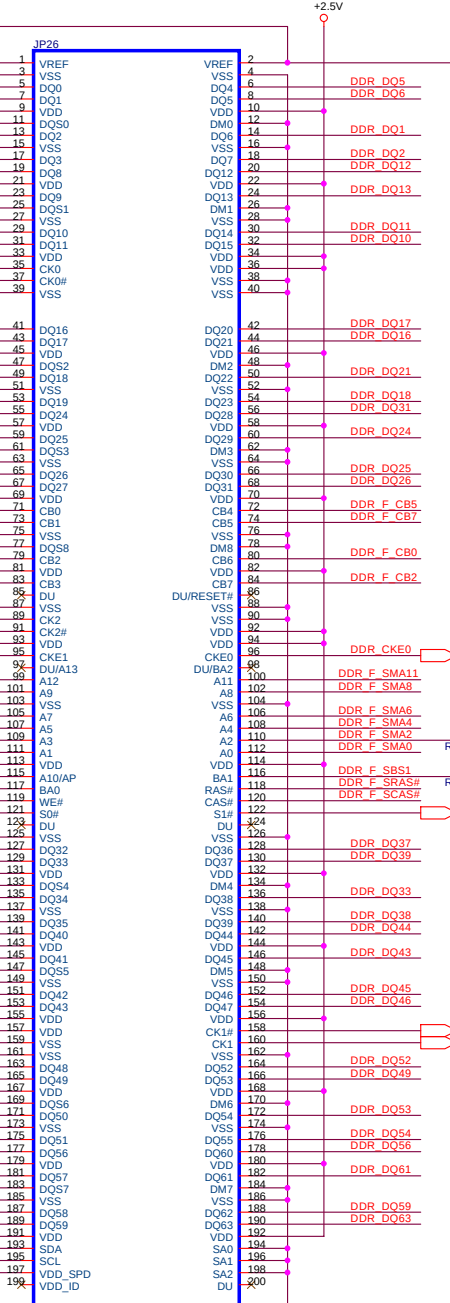
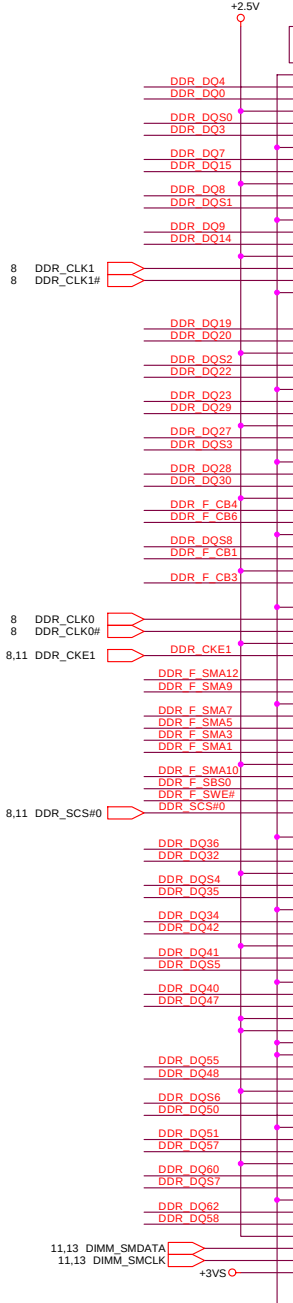
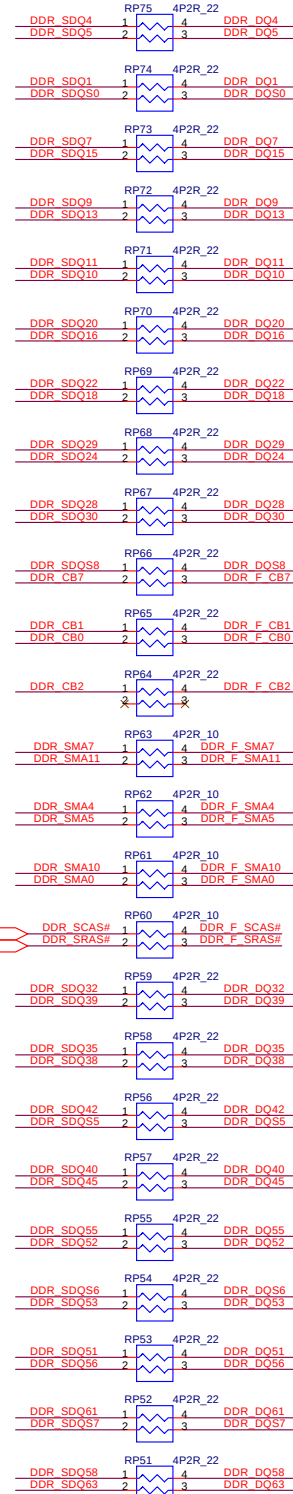
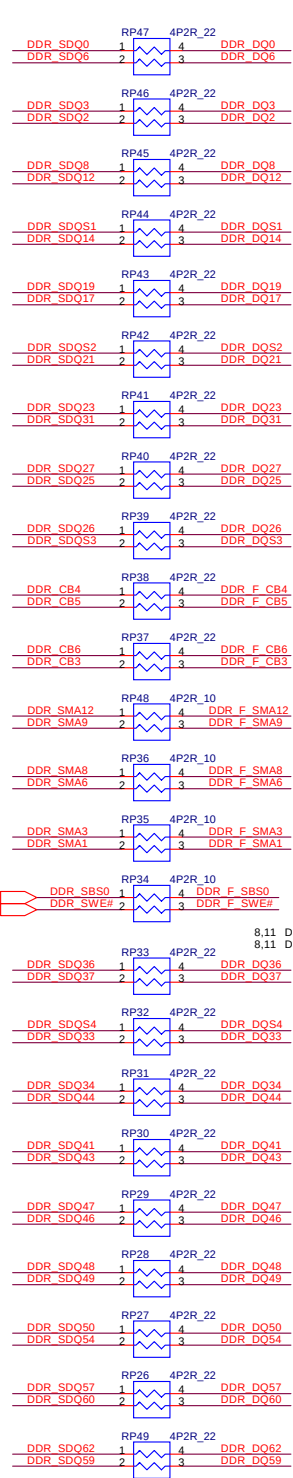


Layout note : Hub-Link
Distribute as close as possible
to MCH Processor Quadrant.(between VCCHL and VSS pin)



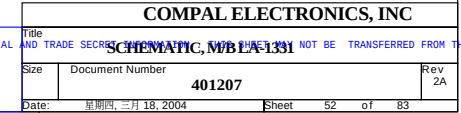
Layout note : DDR Memory interface
Distribute as close as possible
to MCH Processor Quadrant.(between VCCSM and VSS pin)



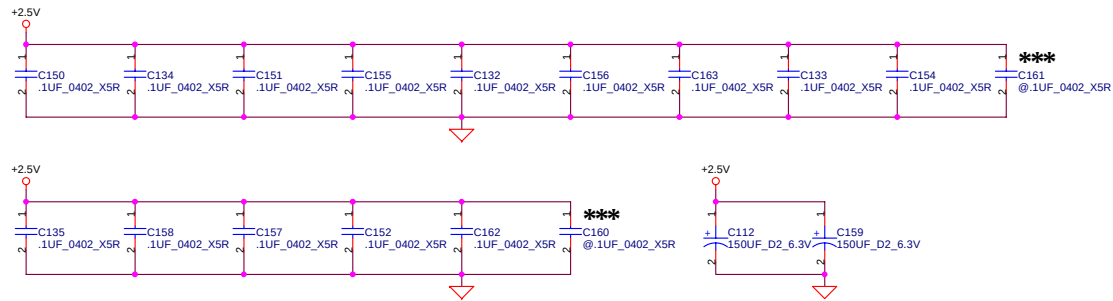


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Size			
Document Number			
401207			
Date			
Rev			
2A			
Date			
Sheet			
51 of 83			



Layout note :
Distribute as close as possible
to DDR-SODIMM.



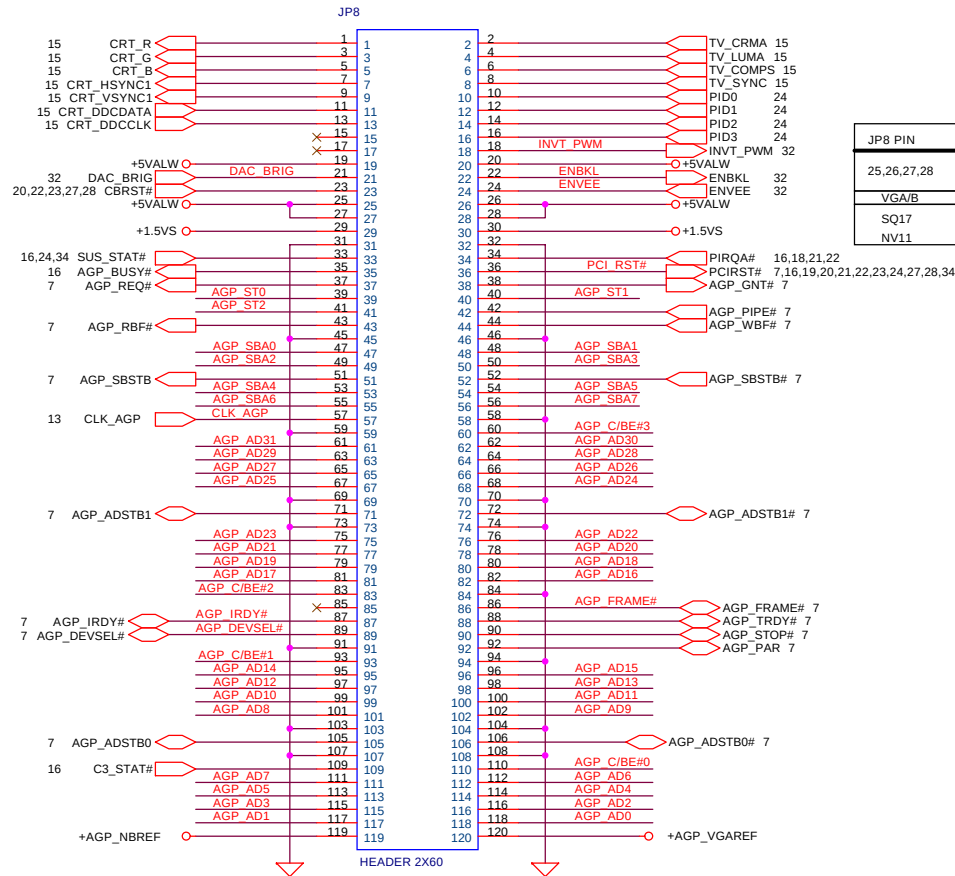
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



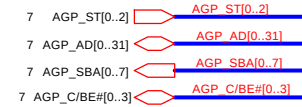
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Title		SCHEMATIC, MBLA-E31	
Size	Document Number		Rev
	401207		2A
Date:	星期四, 三月 18, 2004		Sheet 53 of 83

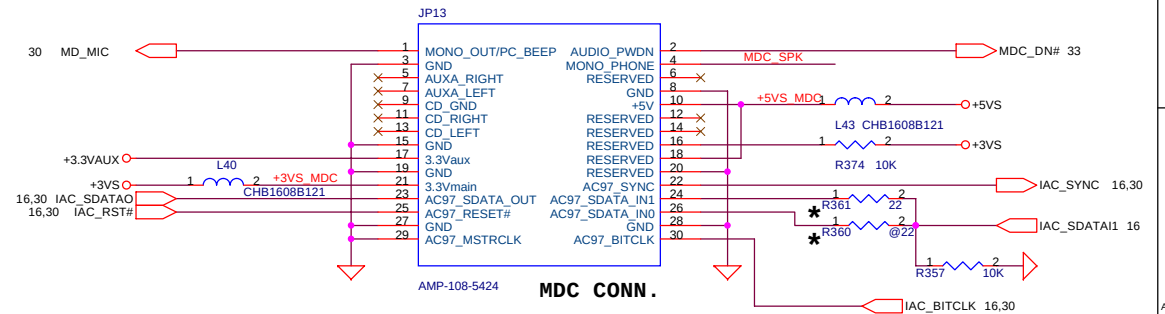
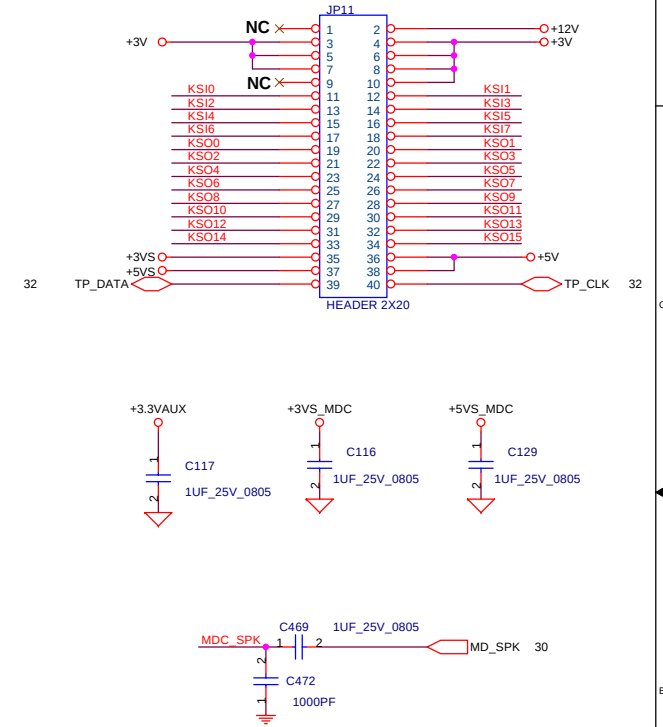
AGP CONN.



JP8 PIN	ACL10	ATL02/ACL00
25,26,27,28	+5VALW	+1.5V
VGA/B		
SQ17	V	X
NV11	V	V



Int. Keyboard CONN.



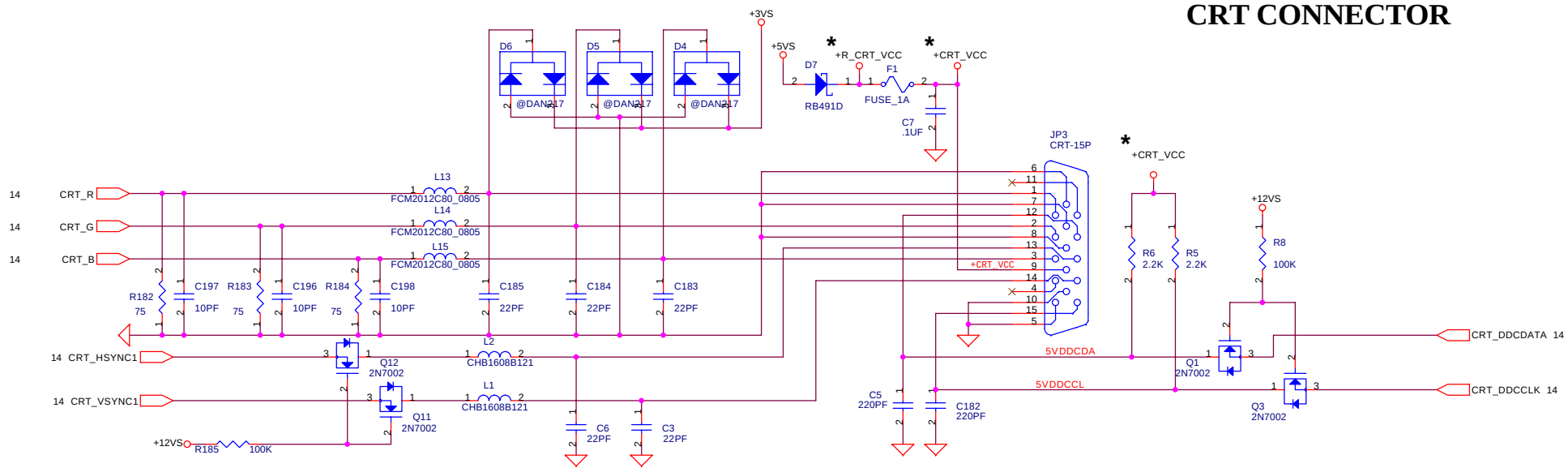
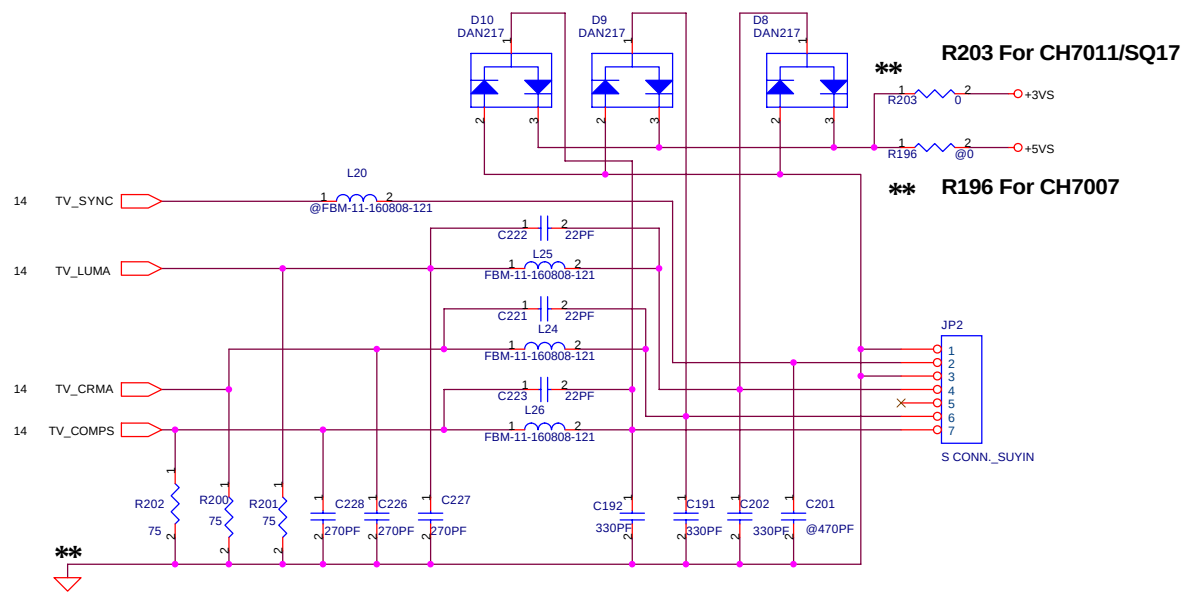
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Date: 星期三, 三月 18, 2004 Sheet 55 of 83

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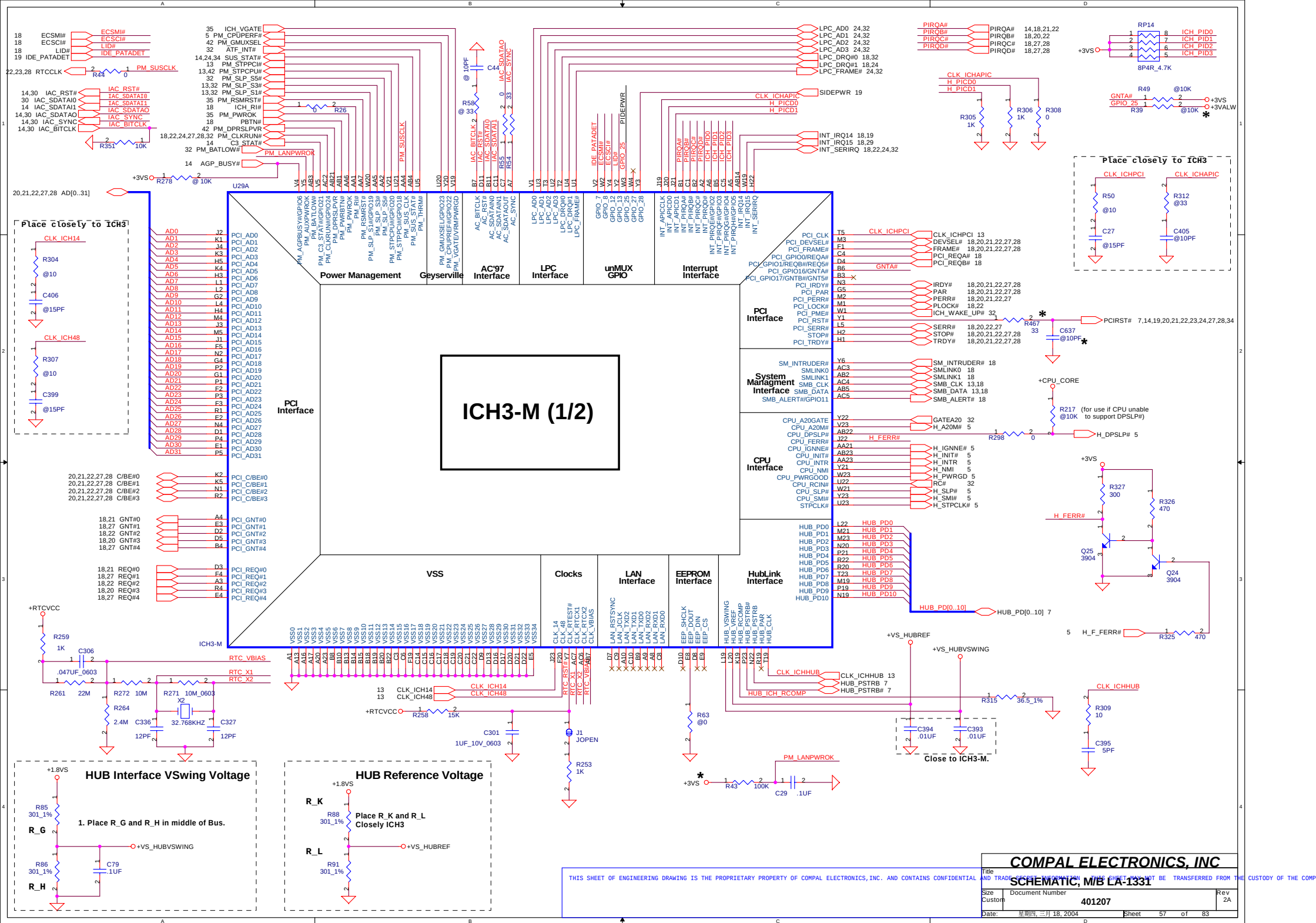
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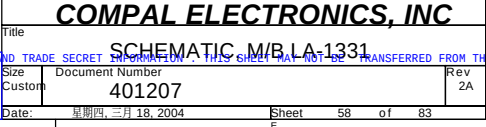
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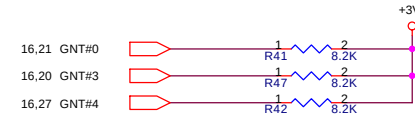
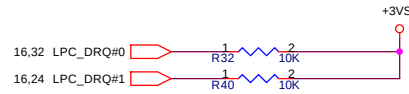
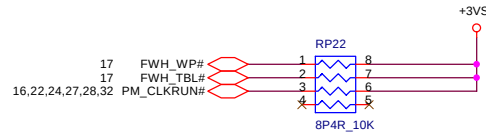
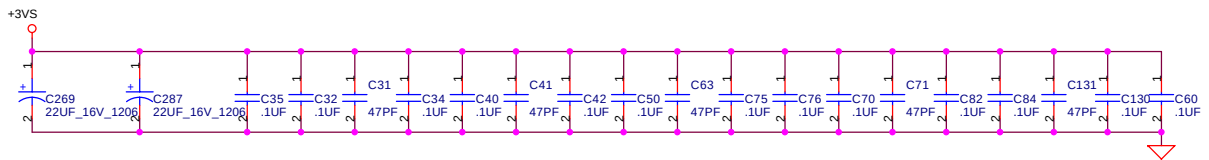
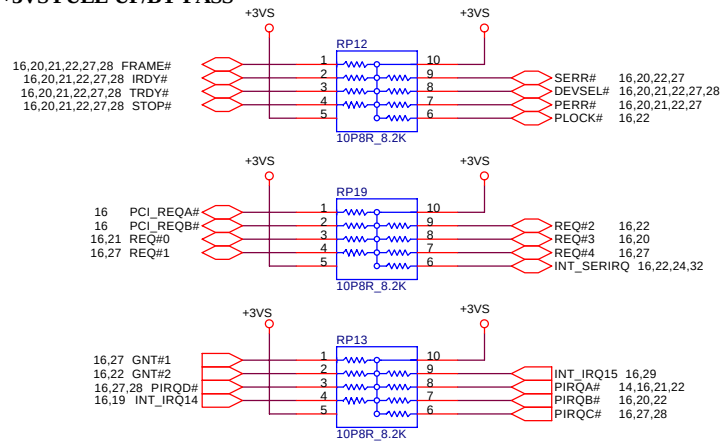
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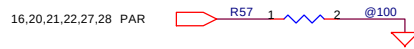




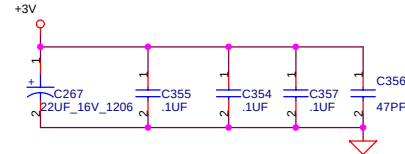
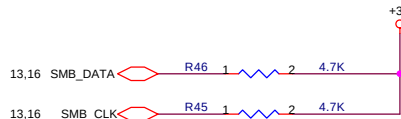
+3VS PULL-UP/BY-PASS



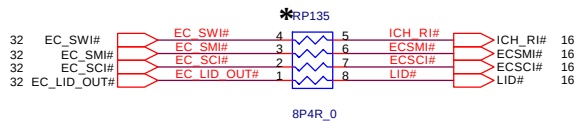
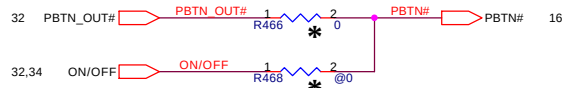
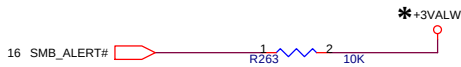
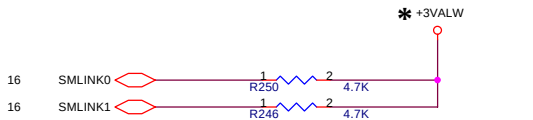
+3VALW PULL-UP



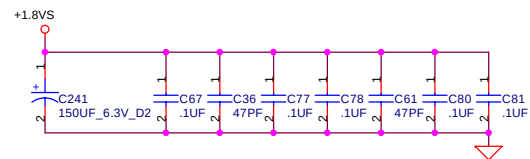
+3V PULL-UP/BY-PASS



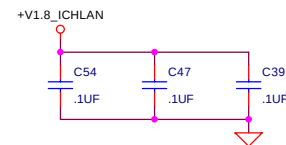
+RTCVCC PULL-UP



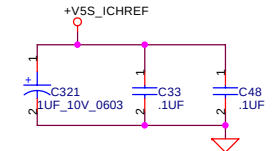
+1.8SV BY-PASS



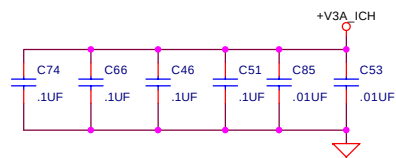
+V1.8S_ICHLAN BY-PASS



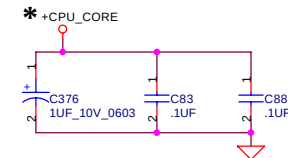
+V5S_ICHREF BY-PASS



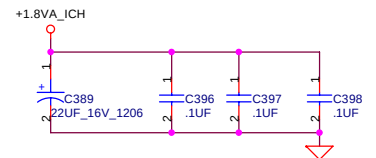
+V3A_ICH BY-PASS



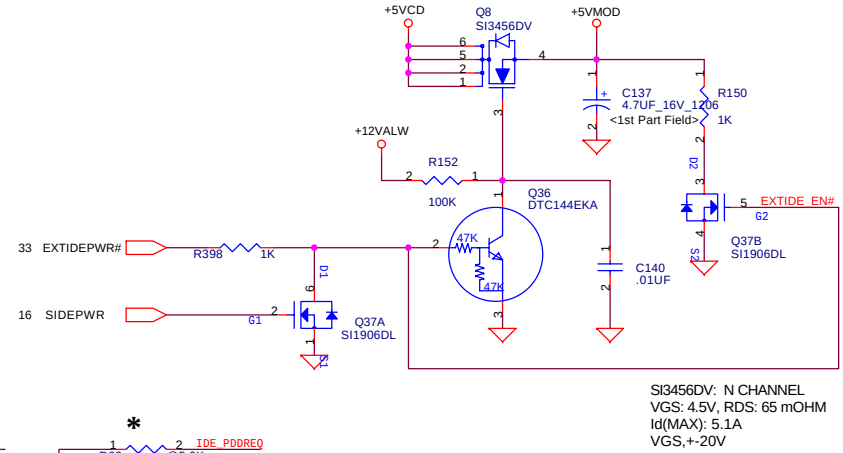
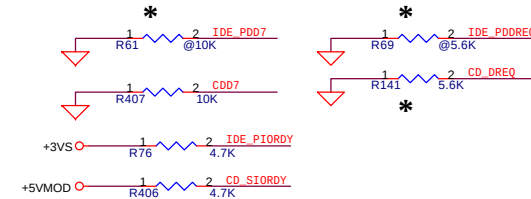
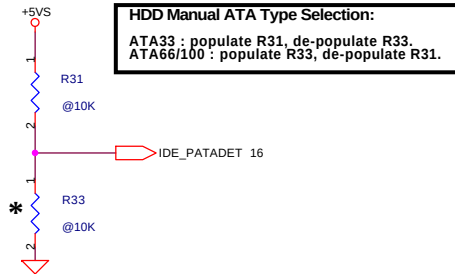
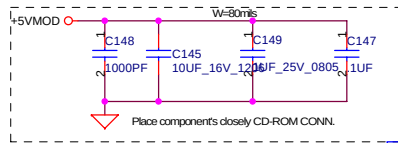
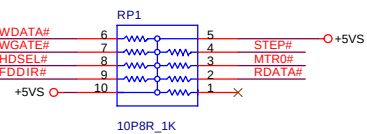
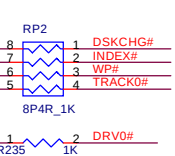
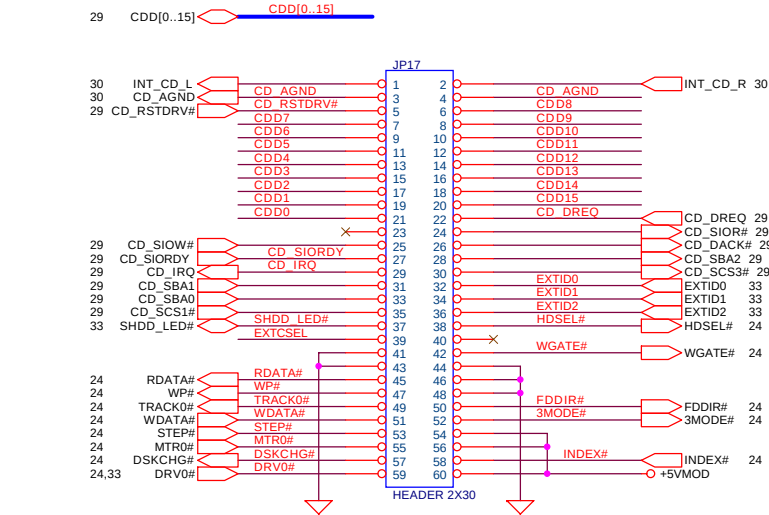
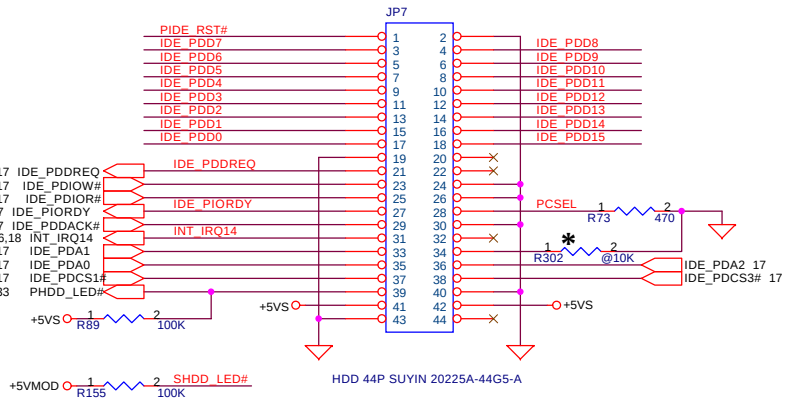
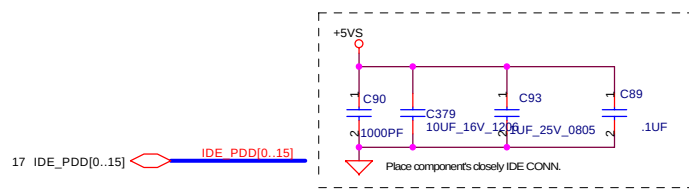
+CPU_CORE BY-PASS



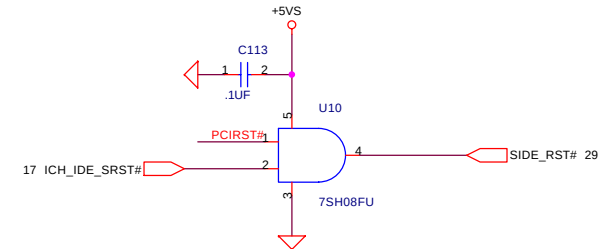
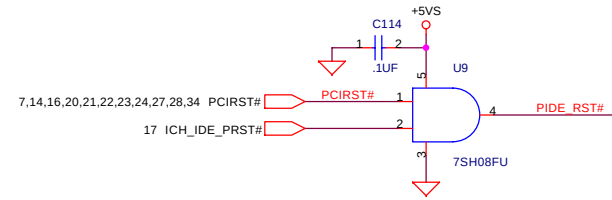
+1.8VA_ICH BY-PASS



IDE,CD-ROM Module CONN.



SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+-20V

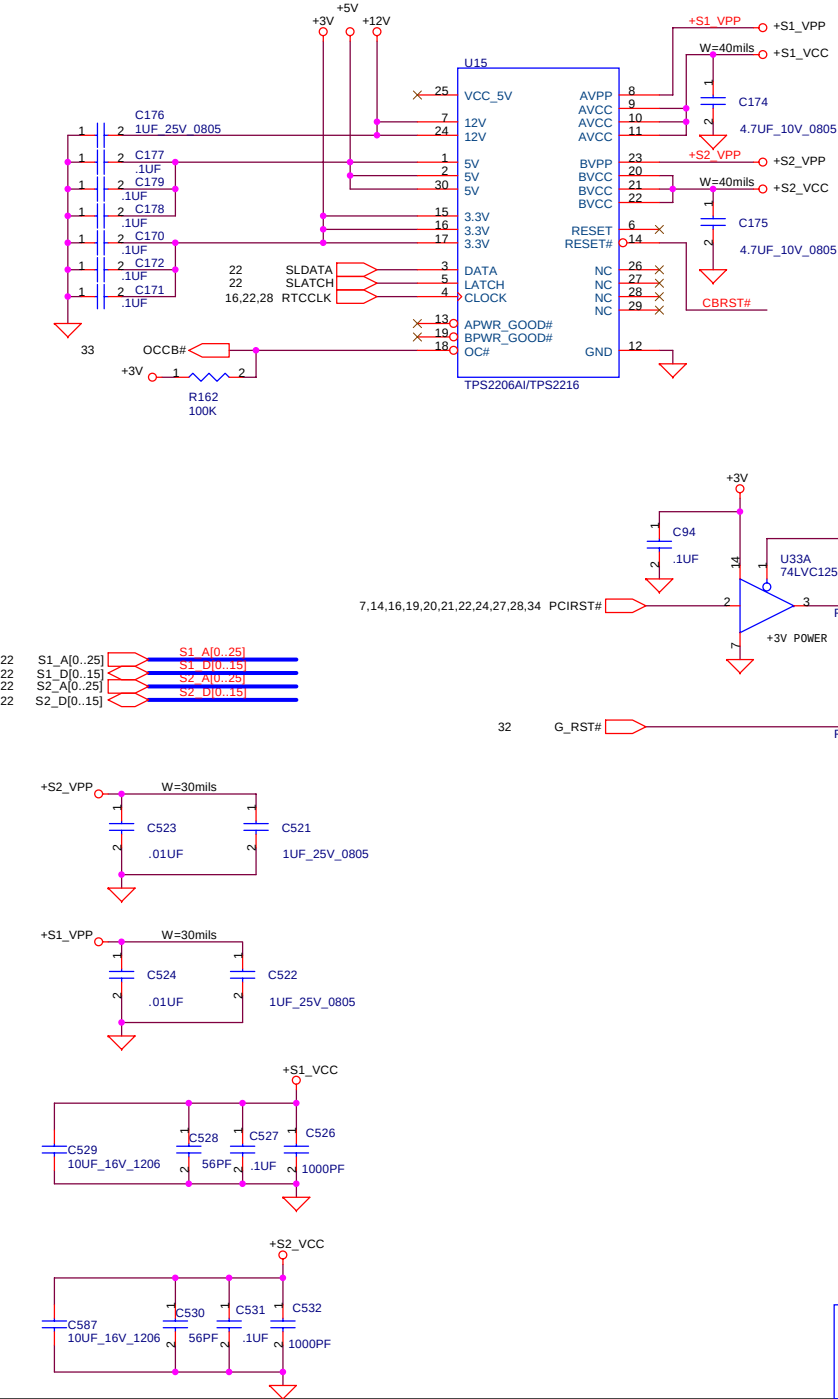


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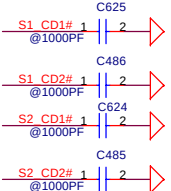
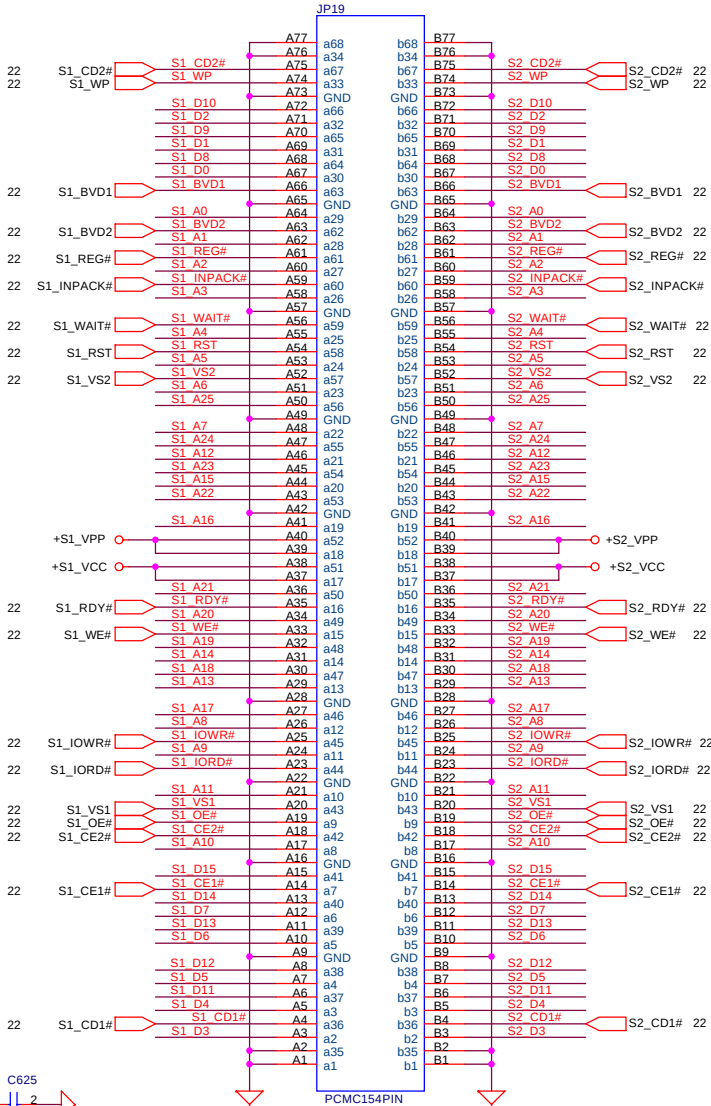
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Title	SCHEMATIC, M/B LA-1331	
Size B	Document Number	Rev 2A
	401207	
Date:	星期四, 三月 18, 2004	Sheet 60 of 83



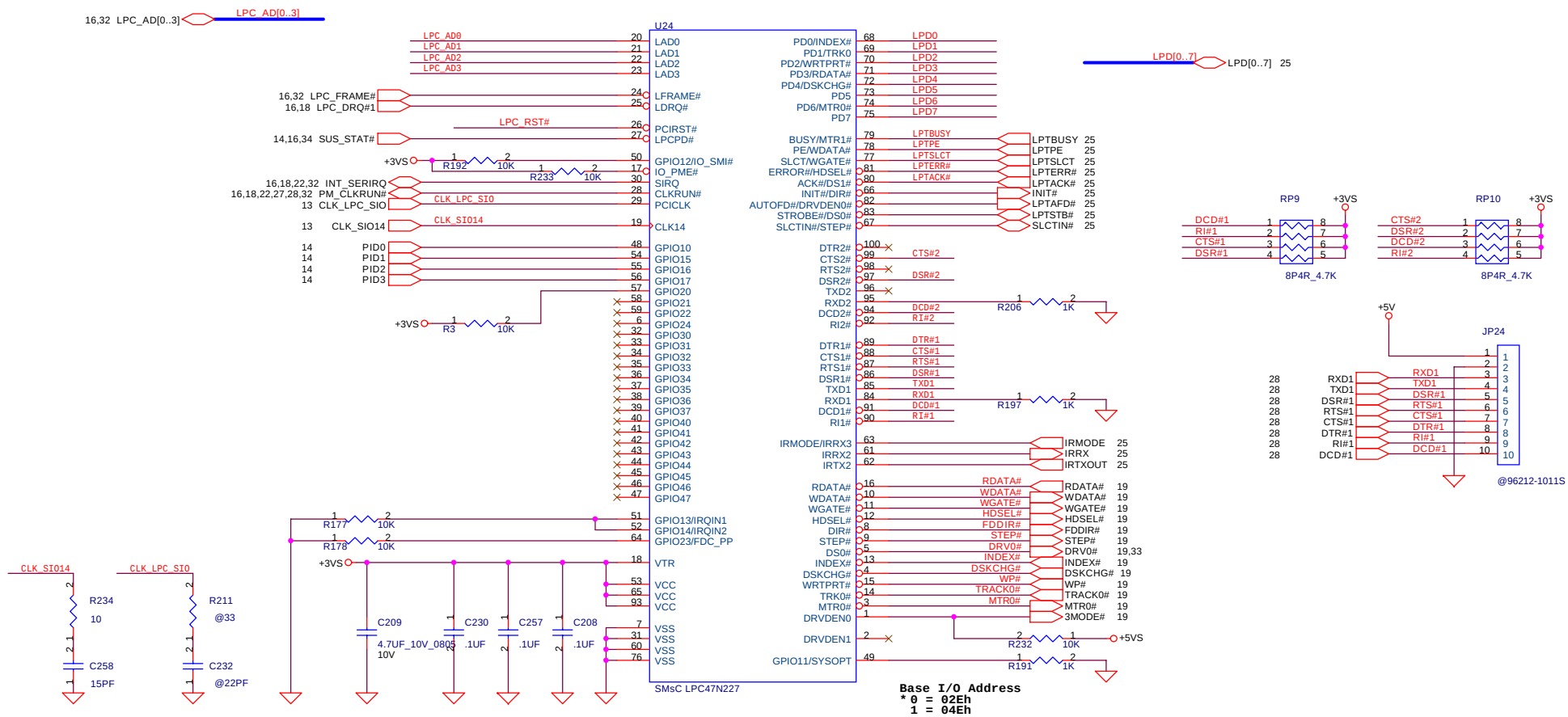
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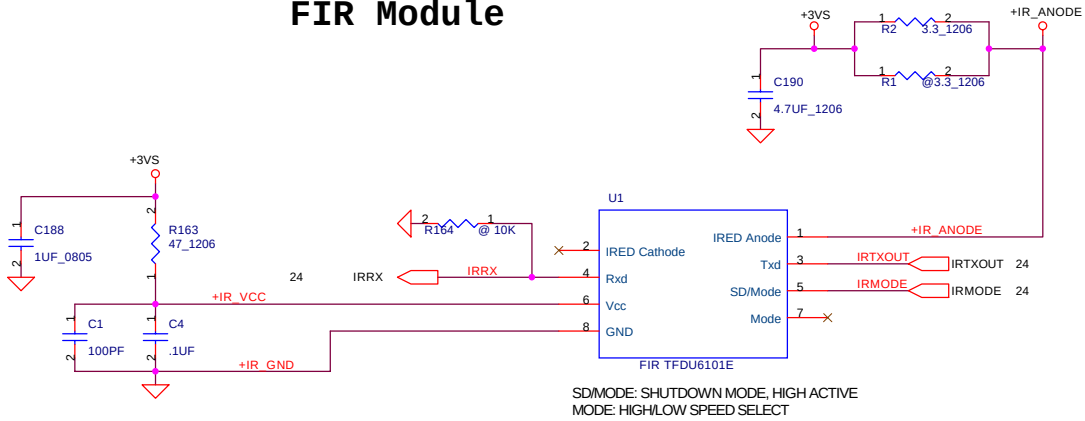
CARDBUS
SOCKET



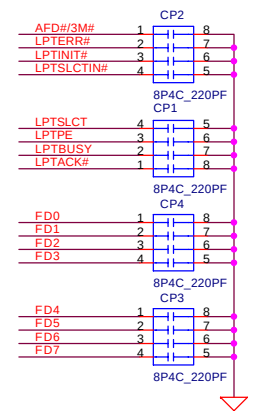
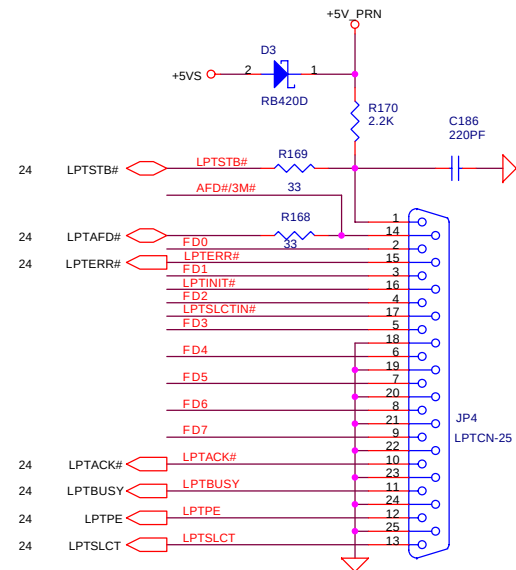
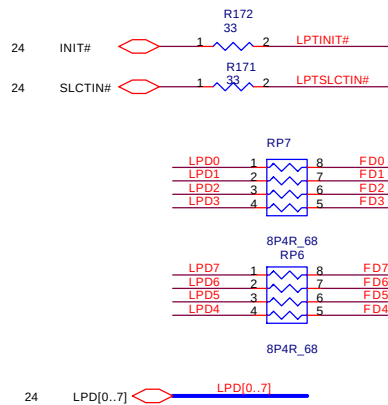
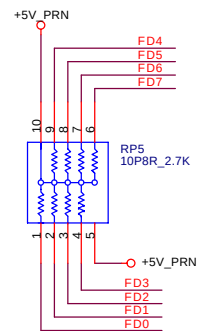
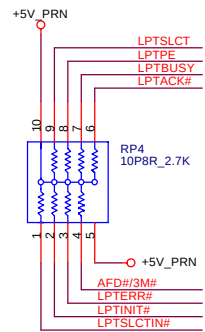
SUPER I/O SMsC FDC47N227



FIR Module



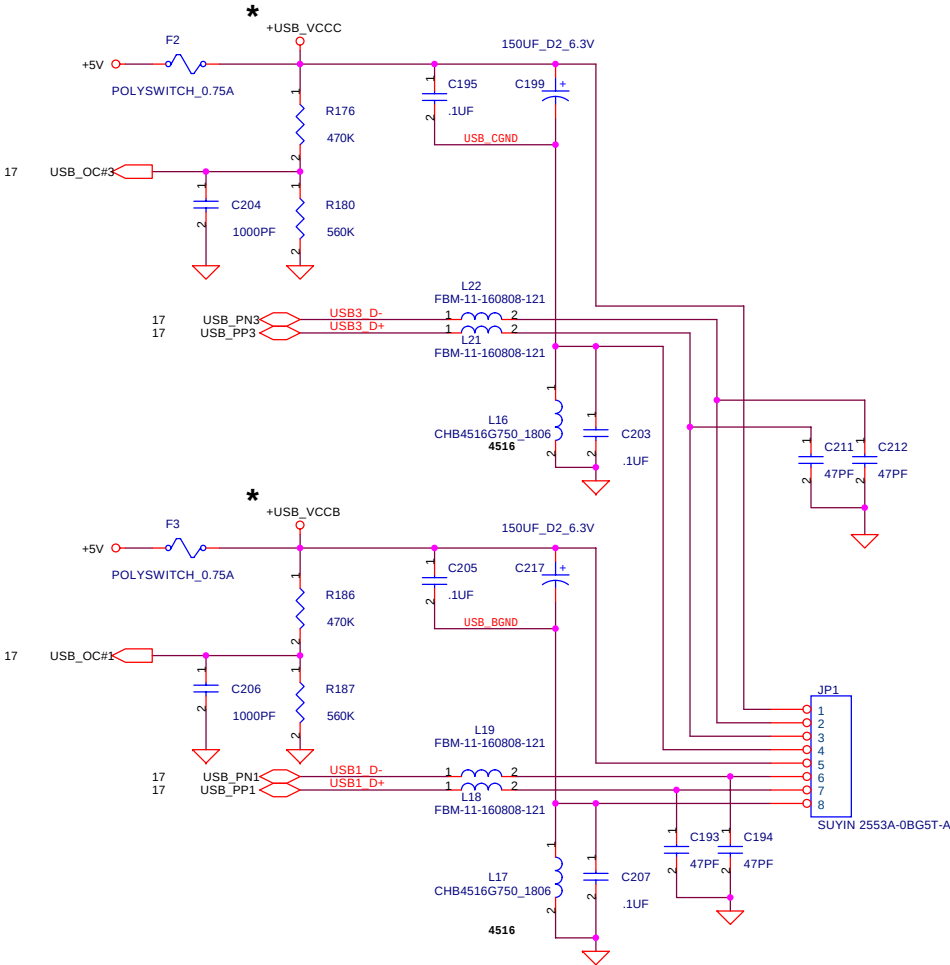
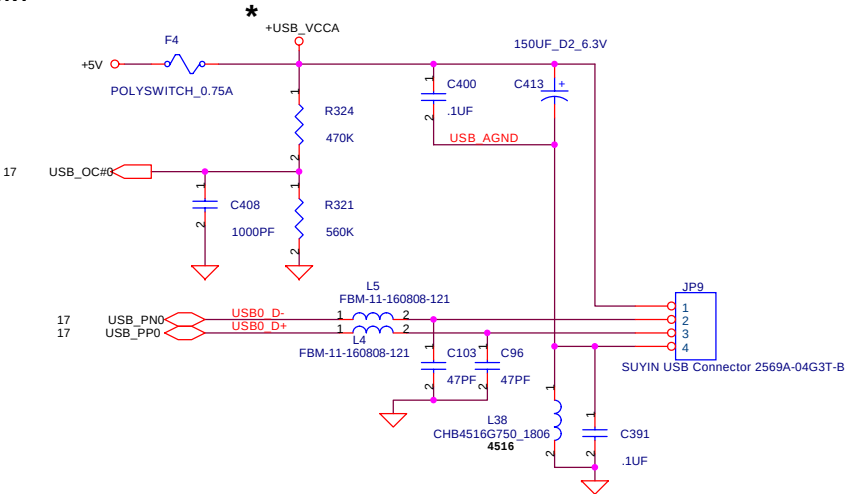
PARALLEL PORT



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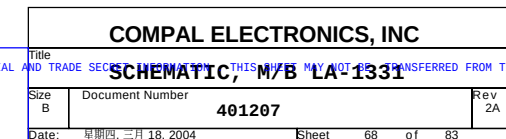
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Title			
SCHEMATIC, M/B LA-1331			
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Document Number			Rev
401207			2A
Date		Sheet	
星期四, 三月 18, 2004		66 of 83	

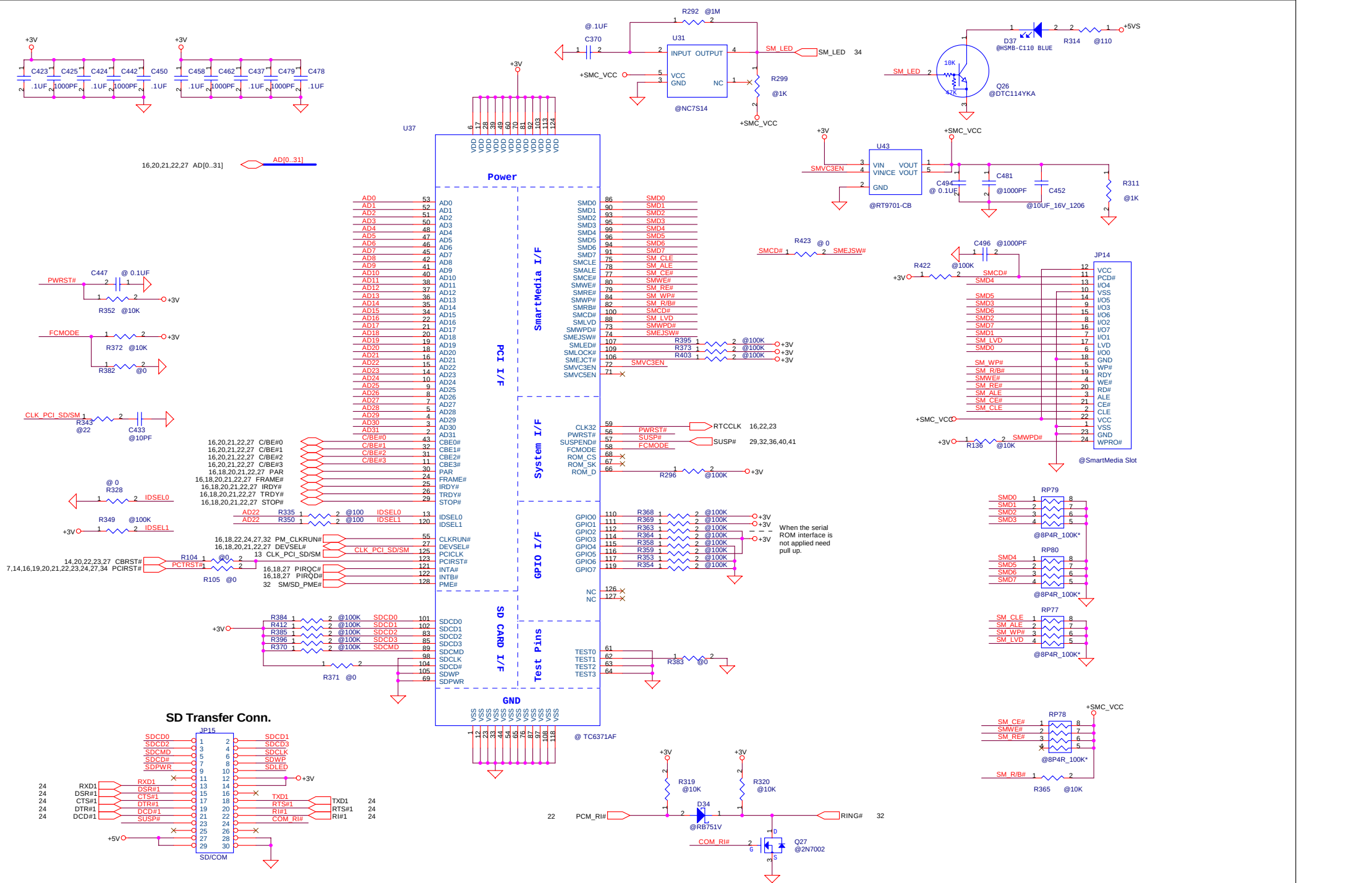
USB PORT



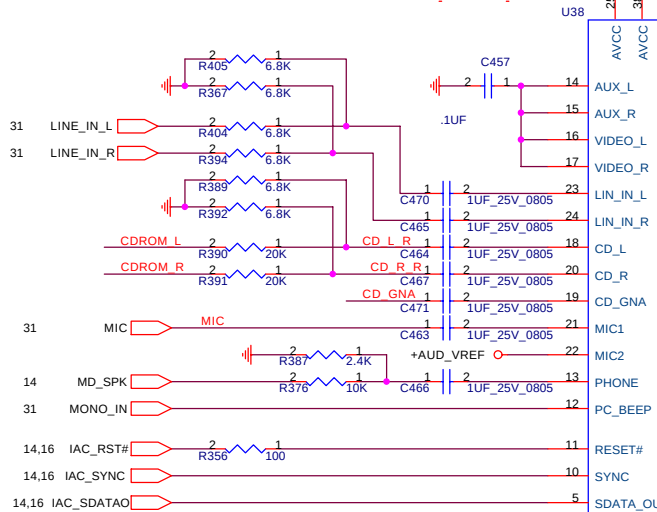
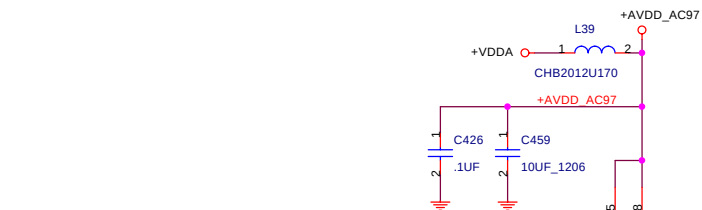
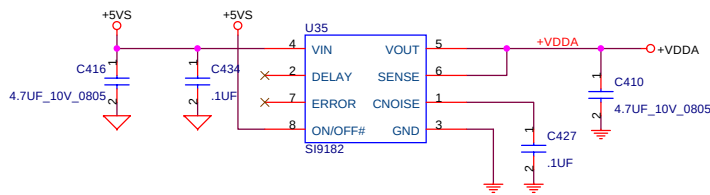
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Title			
SCHEMATIC, M/B LA-1331			
Size B	Document Number		Rev 2A
	401207		
Date: 星期四, 三月 18, 2004	Sheet 67 of 83		

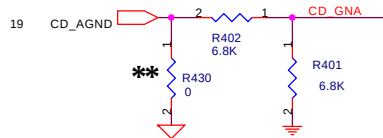




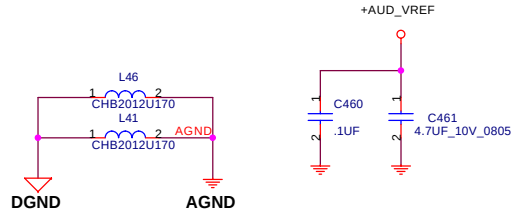
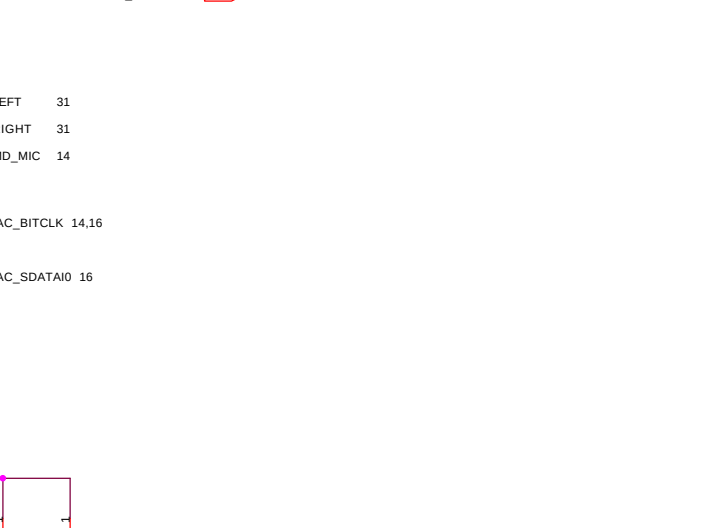
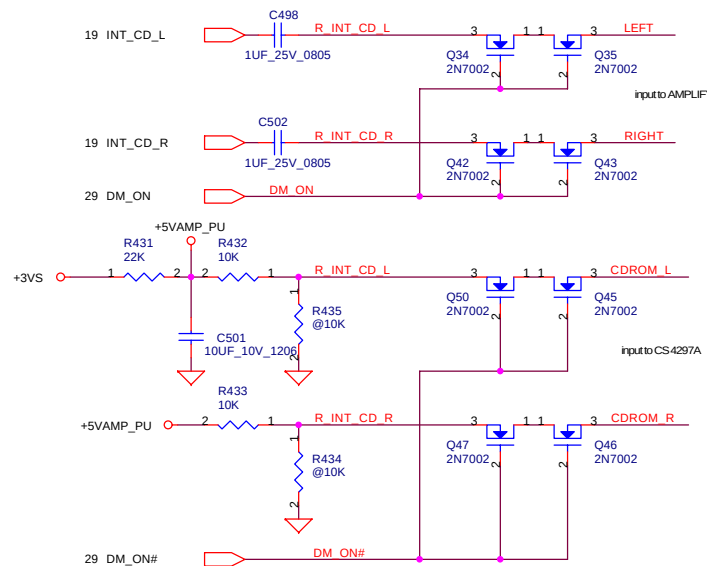
AC97 Codec



R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

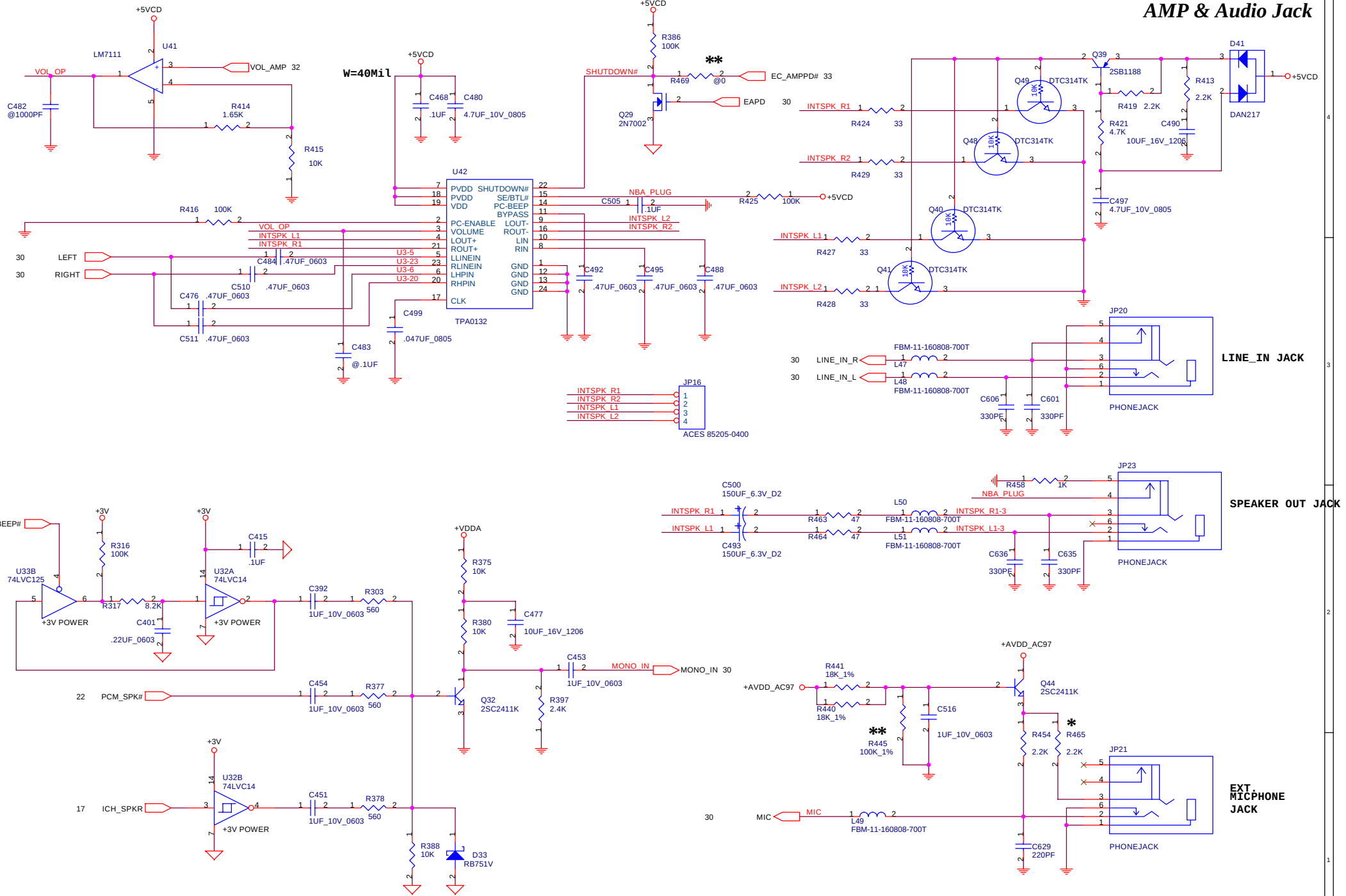


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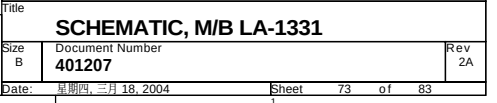
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SCHEMATIC, M/BLA-1331			
Size B	Document Number	Rev 2A	
	401207		
Date:	星期四, 三月 18, 2004	Sheet	71 of 83

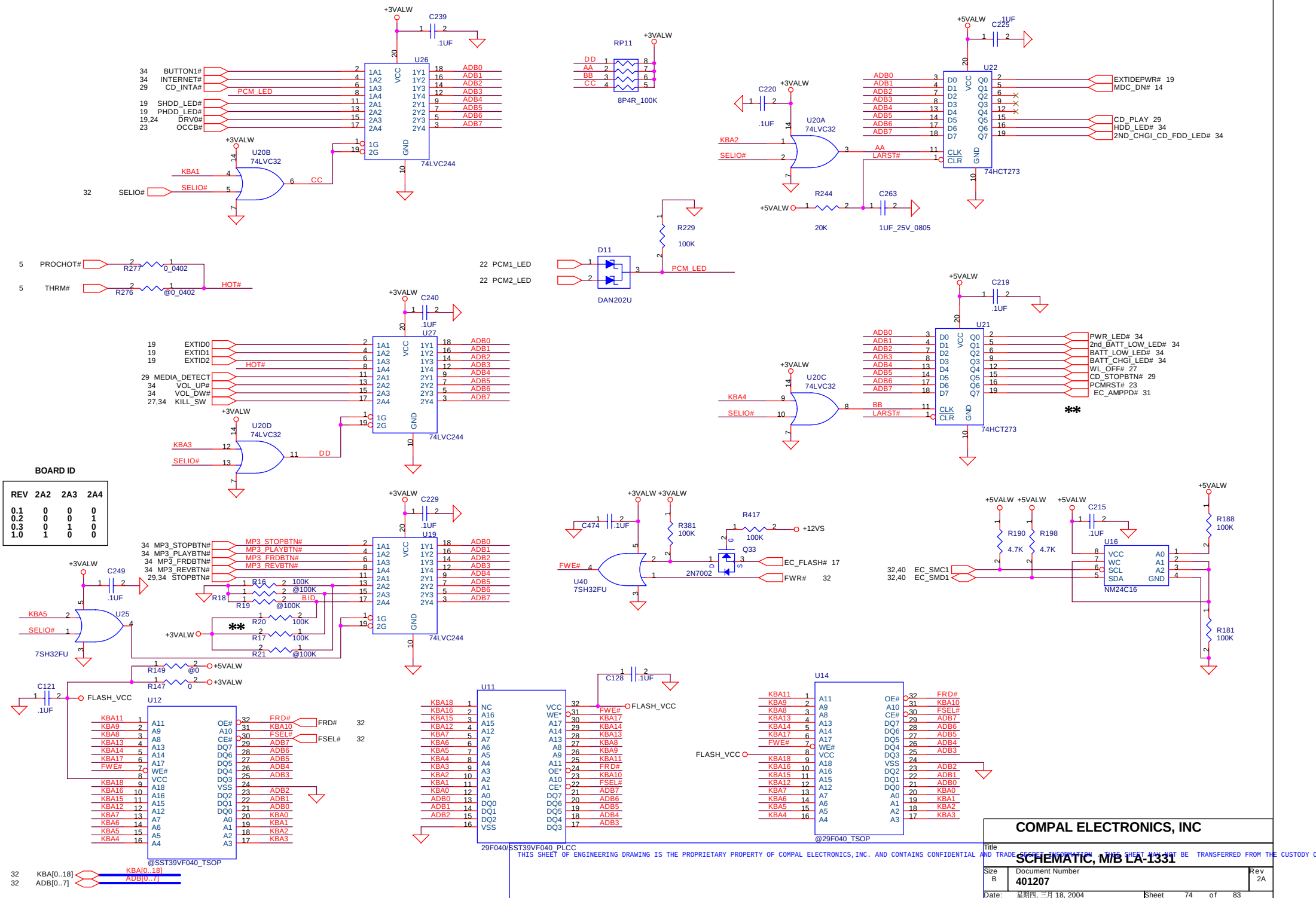
AMP & Audio Jack

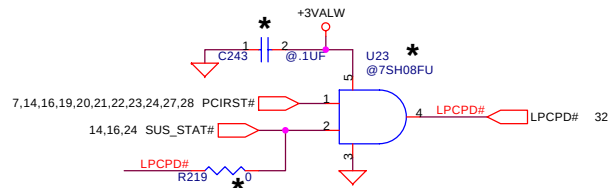
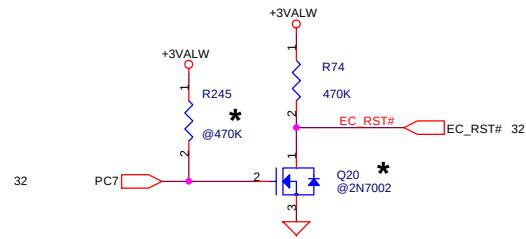


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Size	Document Number	Rev	
B	401207	2A	
Date:	星期四, 三月 18, 2004	Sheet	72 of 83

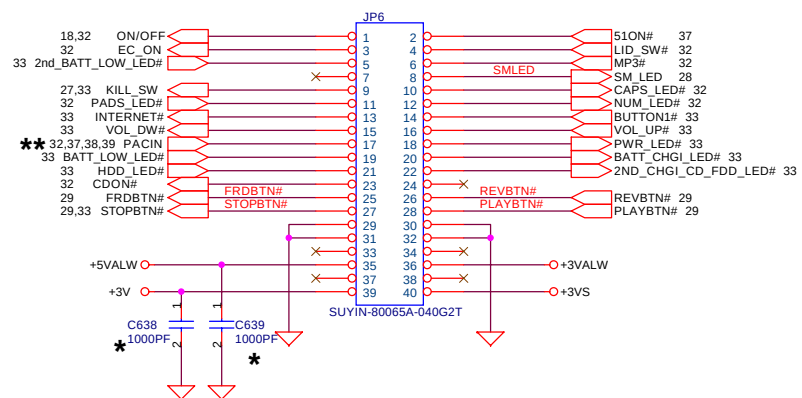
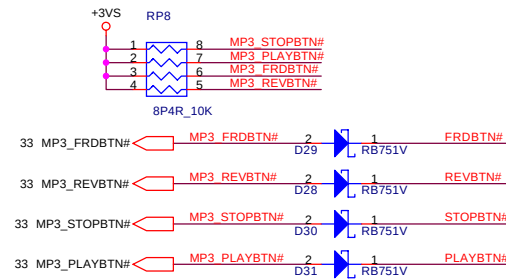
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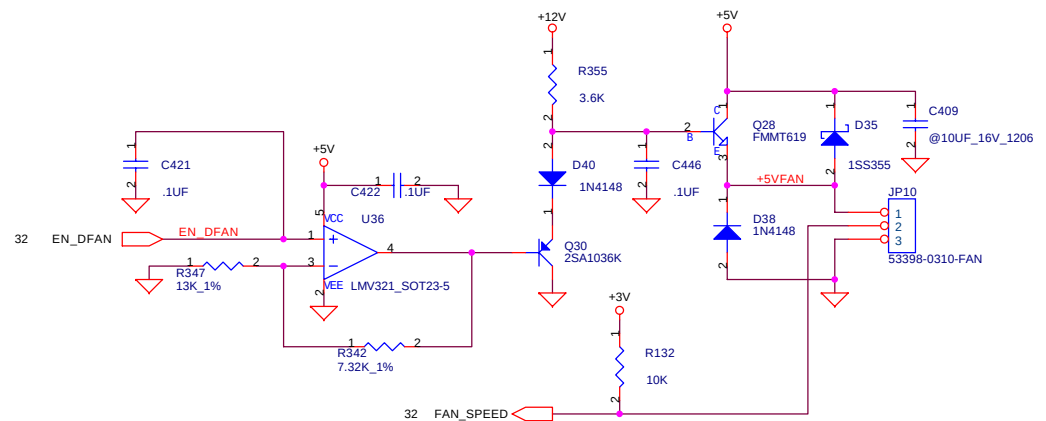




For PC87591 REV 0.A Only



FAN CONN.



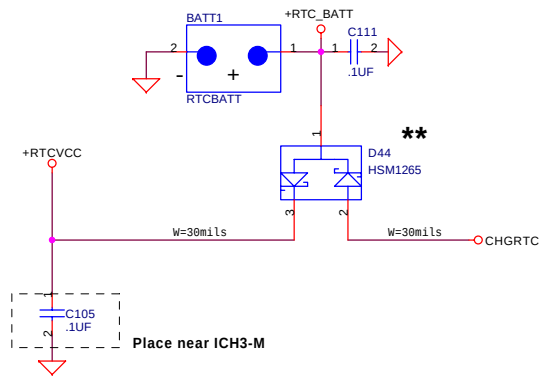
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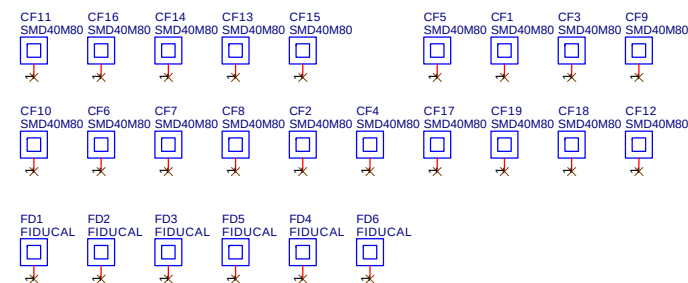
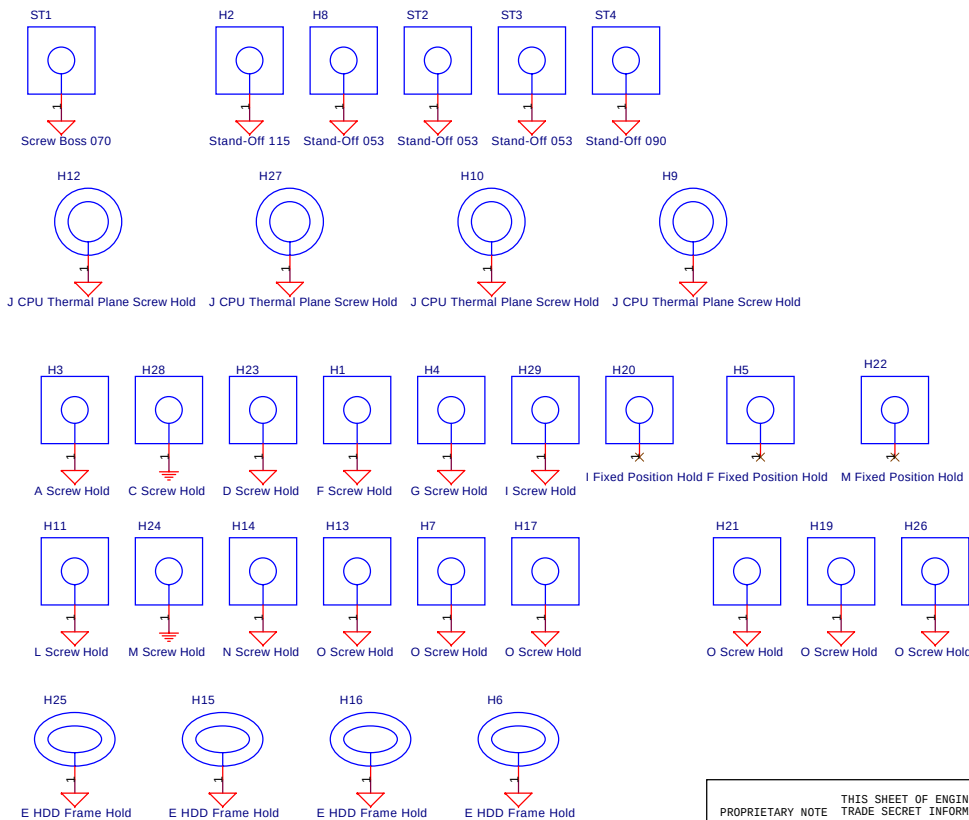
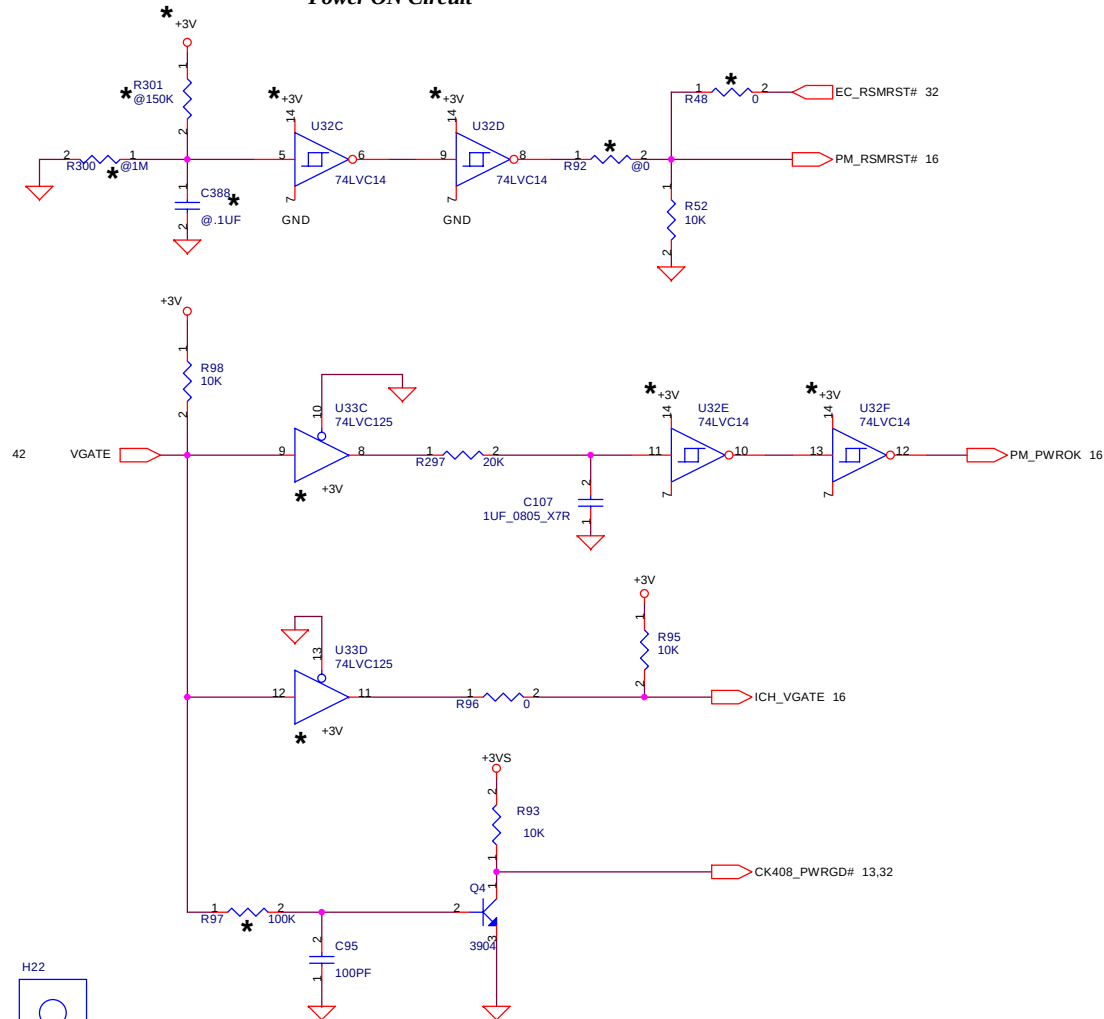
SCHMATIC, M/B LA-1331

Size	Document Number	Rev
B	401207	2A
Date:	星期四, 三月 18, 2004	Sheet 75 of 83

RTC Batt. Connector



Power ON Circuit

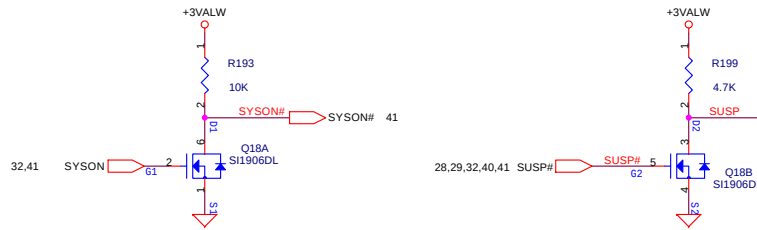
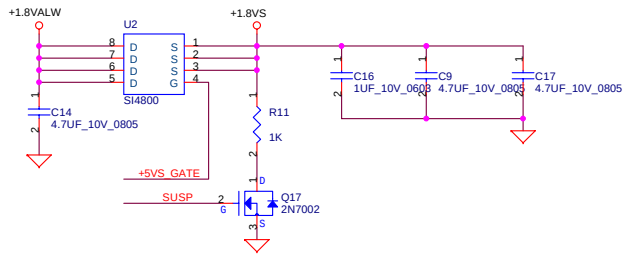


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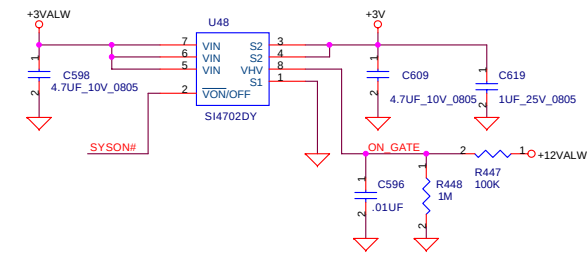
Title		SCHEMATIC, M/B LA-1331	
Size	Document Number	Rev	
Custom	401207	2A	
Date:	星期四, 三月 18, 2004	Sheet	76 of 83

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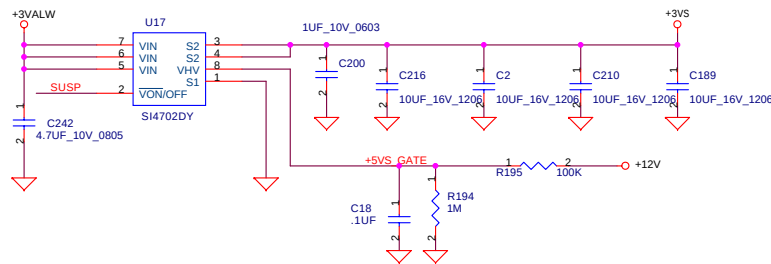
+1.8VALW To +1.8VS Transfer



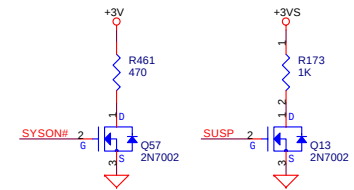
+3VALW To +3V Transfer



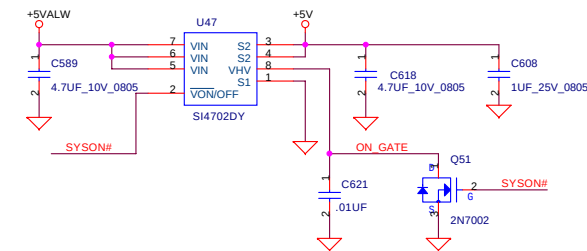
+3VALW To +3VS Transfer



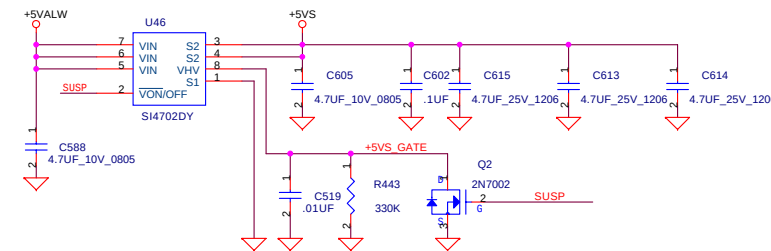
+3V & +3VS Discharge



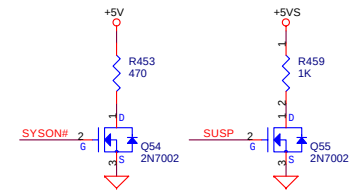
+5VALW To +5V Transfer



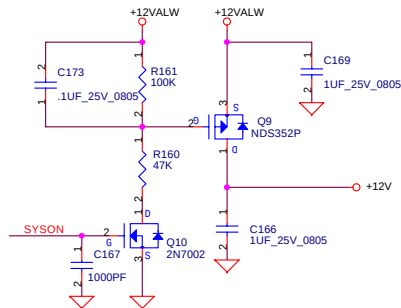
+5VALW To +5VS Transfer



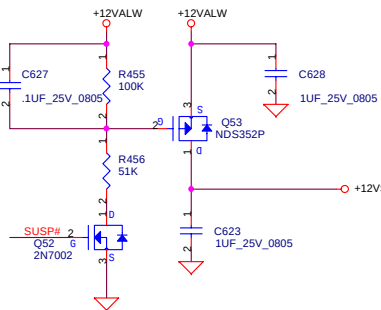
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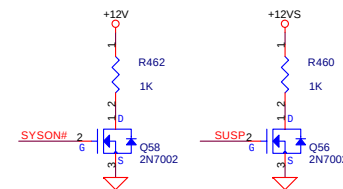
+12VALW To +12V Transfer



+12VALW To +12VS Transfer



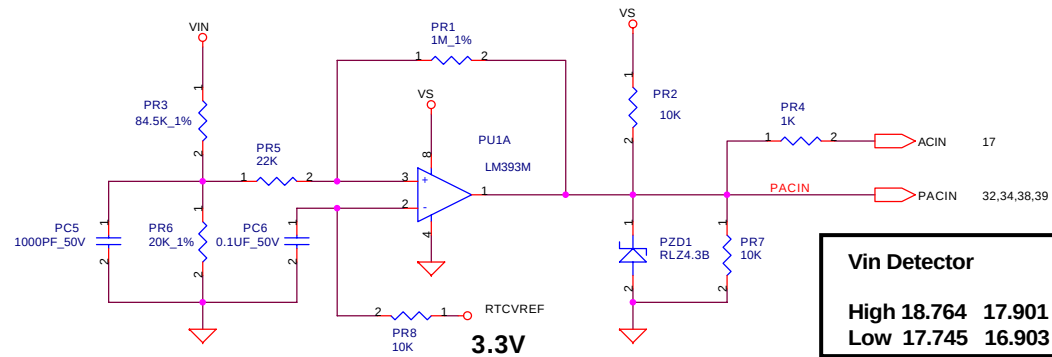
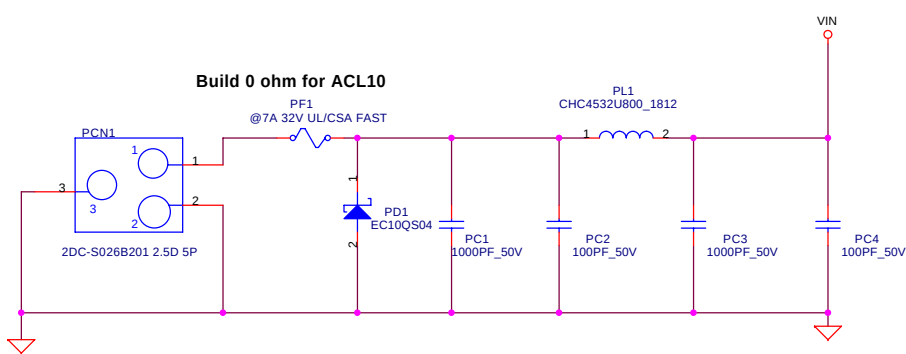
+12V & +12VS Discharge



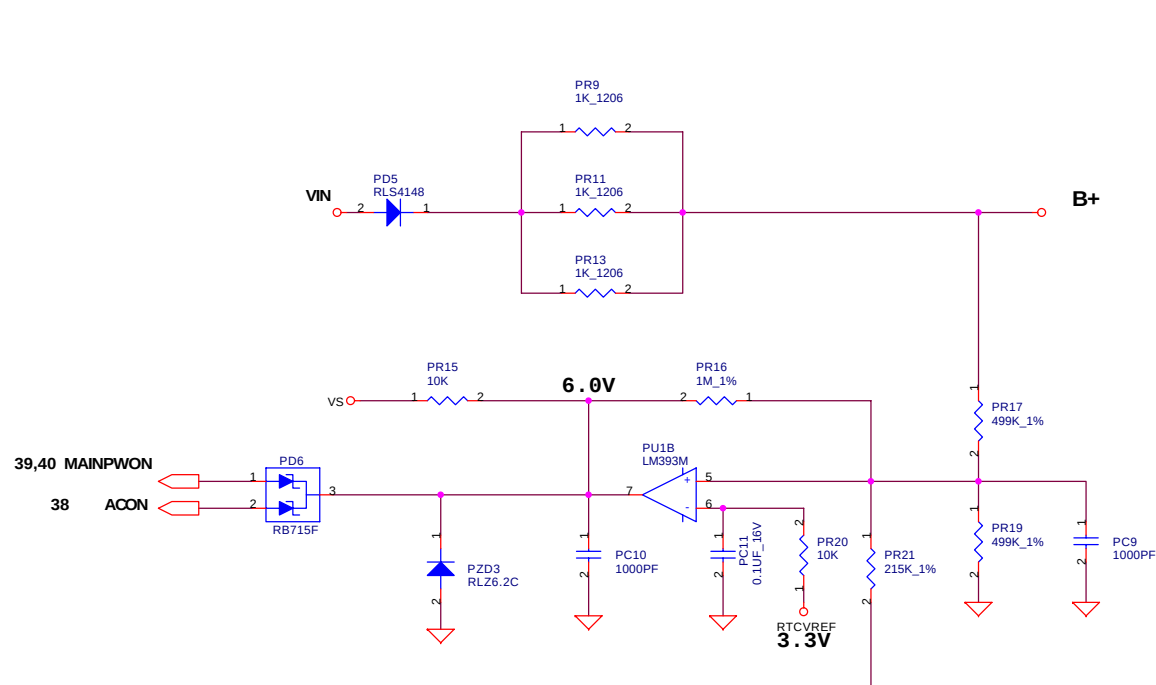
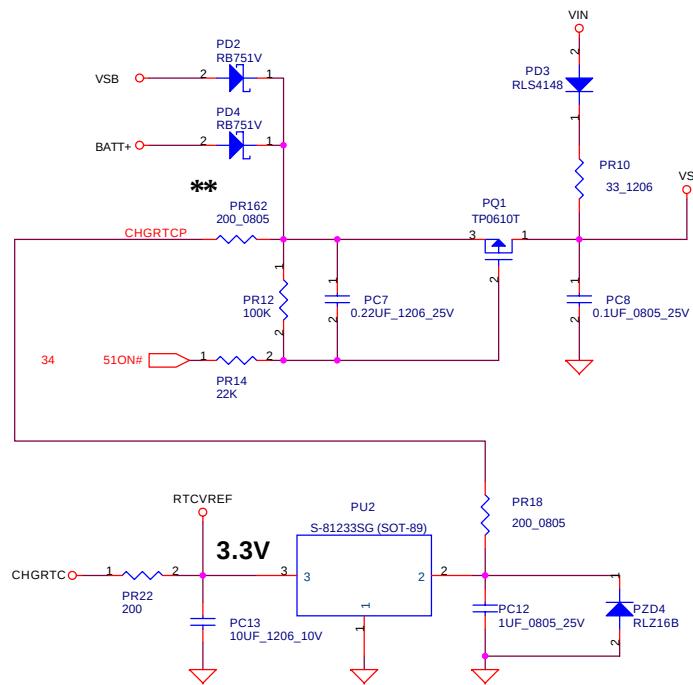
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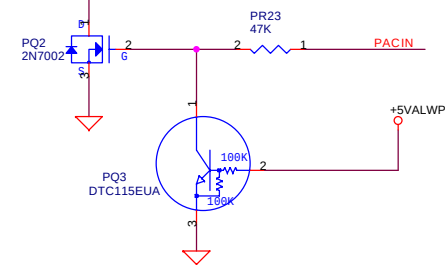
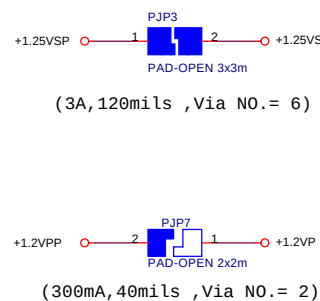
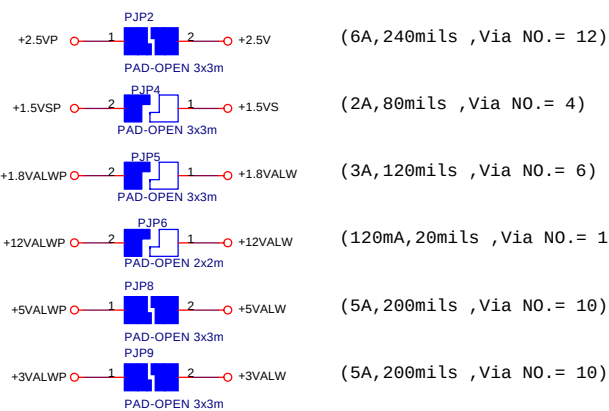
Title			SCHEMATIC, M/B LA-1331
Size	Document Number	Rev	
Custom	401207	2A	
Date:	星期三, 三月 18, 2004	Sheet	77 of 83



Vin Detector		
High	18.764	17.901 17.063
Low	17.745	16.903 16.038

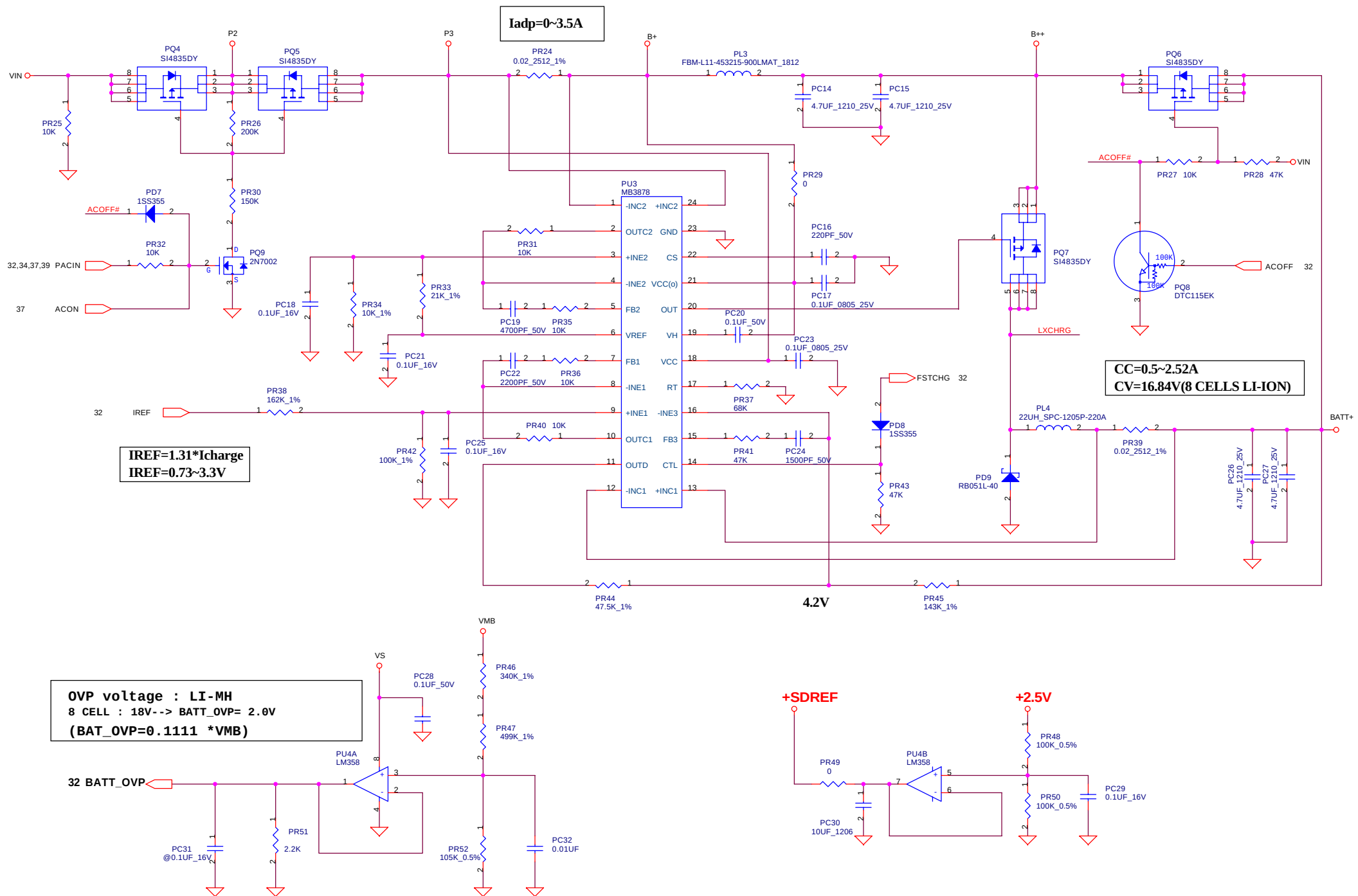


Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20



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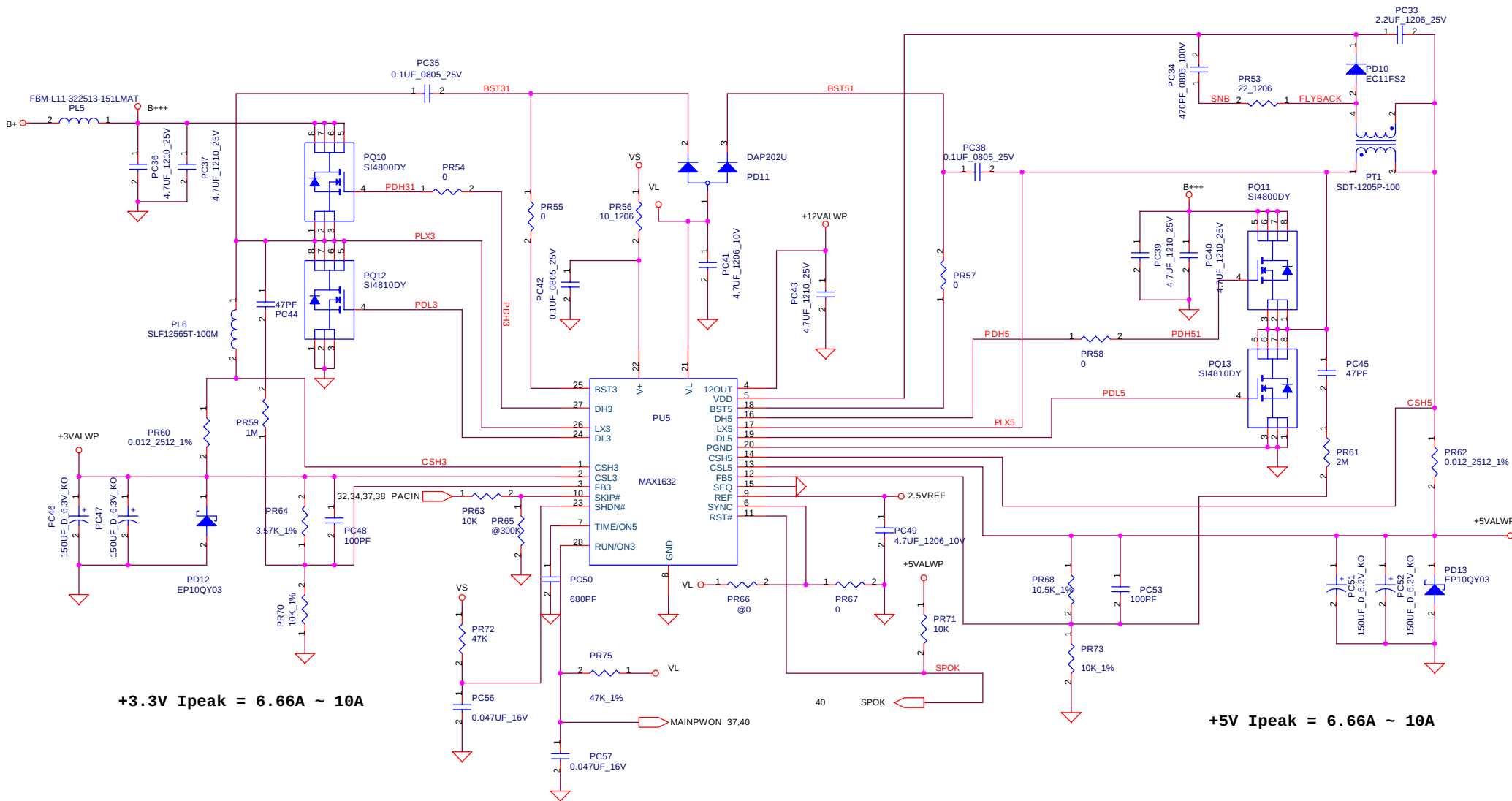
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Title	SCHEMATIC, M/B LA-1331	
Size	Document Number	Rev
B	401207	2A
Date:	星期四, 三月 18, 2004	Sheet 78 of 83



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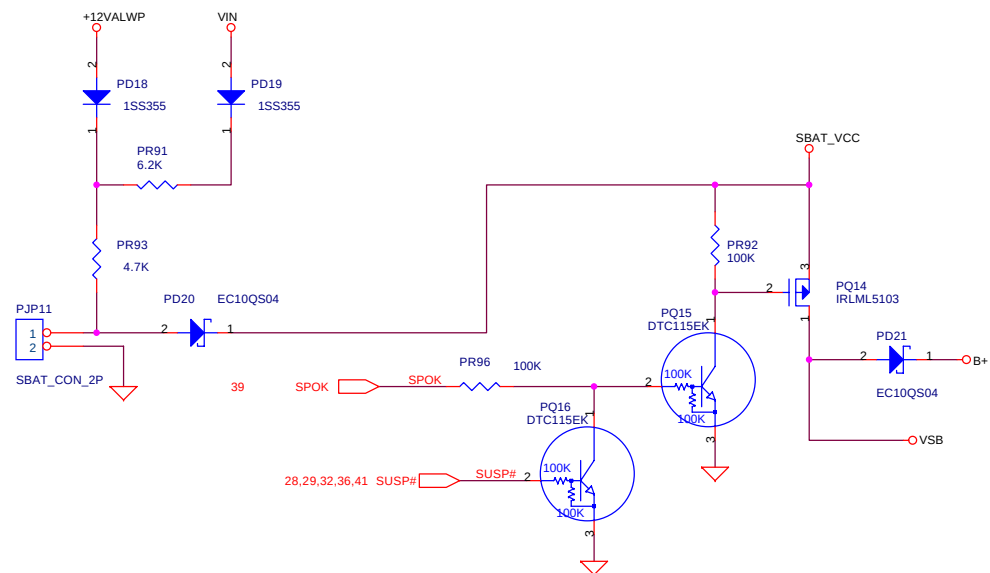
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Size	B	Document Number	401207
Date:	星期三, 三月 18, 2004	Sheet	79 of 83
Rev	2A		



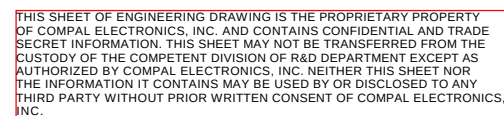
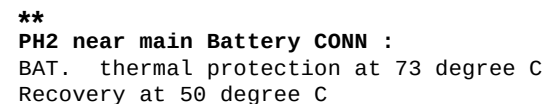
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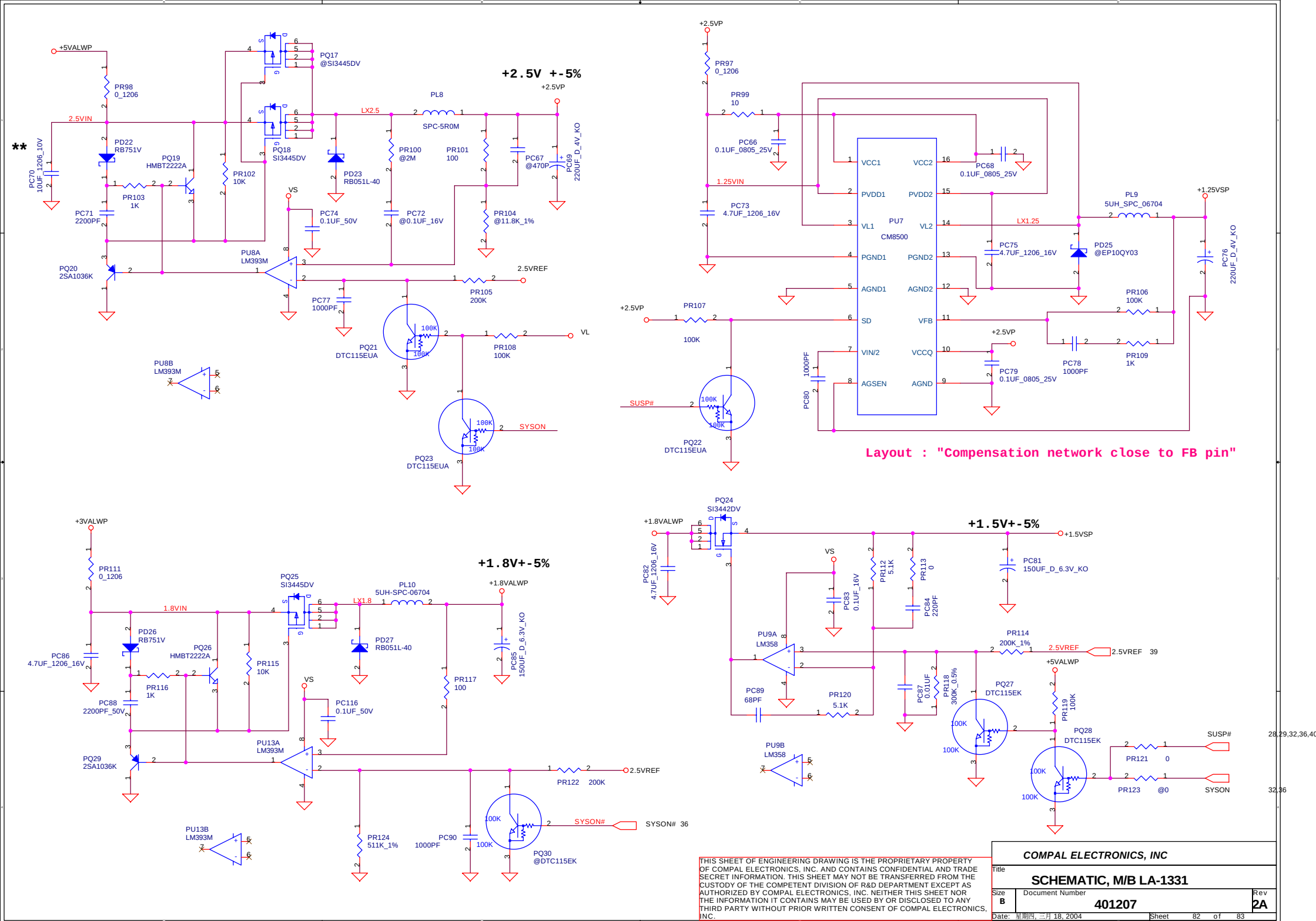
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Title		SCHEMATIC, M/B LA-1331	
Size	B	Document Number	401207
Date:	星期四, 三月 18, 2004	Sheet	80 of 83
Rev	2A		



PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C





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